Title **Silicon chips characterization**

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AHEAD

DOCUMENT CHANGE RECORD

Issue	Date	Changed Section	Description of Change

Abbreviations and acronyms

Item	Meaning
TES	Transition Edge Sensor
CryoAC	Cryogenic Anti Coincidence
X-IFU	X-ray Integral Field Unit
SQUID	Superconducting Quantum Interference Device
FLL	Flux Locked Loop
ADR	Adiabatic Demagnetization Refrigerator
NTD	Neutron Transmutation Doped

Applicable Documents

[AD#]	Doc. Reference	Issue	Title

Reference Documents

[RD#]	Doc. Reference	Issue	Title
[RD1]	AHEAD-WP6-REP-004-2016		WP6: CryoAC trade-off
[RD2]	Proceedings of the SPIE, Volume 10699, id. 106994T (2018)		The Cryogenic Anticoincidence Detector for ATHENA X-IFU: Preliminary test of AC-S9 towards the Demonstration Model

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1 EXECUTIVE SUMMARY

The conclusion of our last reporting period was that the work we planned and started for CD#1 in the AHEAD context was related to selection of high purity Silicon chips (i.e., having different resistivity) in order to comply the energy resolution requirement. Being the CD#1 design [RD1] an optimization of the baseline CryoAC single pixel detector (the main path of the CryoAC technological work is inserted in the X-IFU roadmap that foresees the development of a DM "Demonstration Model"), the main experimental work will be devoted to characterization test of optimized samples.
Thus, the last part of work to be performed as testing activity is related to Silicon chips characterization such as chemical composition and thermal conductivity, whose results could be interesting in designing a spectroscopic CryoAC. This feature can be verified by the single pixel CryoAC detector we are going to develop in the context of the Athena activity, i.e. the DM, whose main requirement are below reported:

- Pixel dimensions (abs. area) → ≤ 10x10 mm^2
- Energy Range → Threshold at 20 keV
- Bath Temperature → 50-55 mK
- Deadtime and VETO → The DT (intrinsic), at first approximation it can be evaluated from the rise-time inside the transition. Not foreseen out-of-band illumination. The VETO (i.e., synchronization between the two detectors) is under discussion/evaluation. For both not performance test

To perform the thermal conductivity test, it has been necessary to produce so-called "test structures". Our test structures activity has mainly involved, and successfully passed the:

- Etching of Silicon wafer to have a high area (1 cm^2) suspended absorber → this has an impact on the fabrication process but also on any structural issue during cool-down procedures
- Characterization of the thermal conductance from the suspended absorber to the Si rim realized by the Si beams, the last being our real thermal bath → this has an impact on both the thermal time constant and the out-of-transition detector DeadTime.

2 "TEST STRUCTURE" FABRICATION

The test structures designed and developed necessary to face an "under control" design and production of the CryoAC single pixel, which we consider as the DM, has been:

- Production of suspended Si absorber

2.1 CryoAC DM-like geometry and thermal conductance "G" made of Si beams

In this activity, we studied the DM silicon beams fabrication process and evaluated different geometries. During this activity, we have understood that the main feature to be investigated in relation to the thermal conductance was the Si resistivity rather than the shape of the beams. Thus, two different beam geometries have been produced. The simple linear beam 1 mm long and 100 µm wide, which is the baseline (Fig. 1) has been produced with the thickness of 260 µm and 500 µm, this geometry is also used to evaluate the thermal conductance versus the Si resistivity. Instead the meander geometry with 100 µm width, 4 mm of total length and 500 µm of thickness has been produced only to test the fabrication performance, as backup solution in case to be necessary reduce the thermal conductance (Fig. 2).

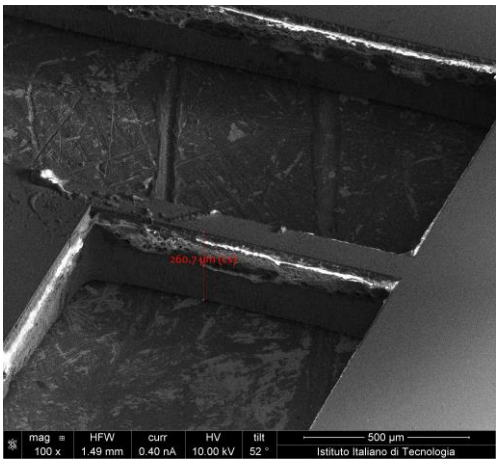

Fig. 1 – Scanning electron miscroscope image of a simple linear silicon beam produced as test.

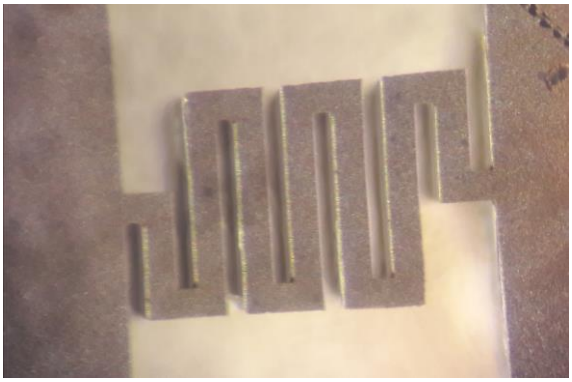

Fig. 2 - Optical image of meander type silicon beam.

To produce these structures, Silicon wafers have been etched using the Bosch process as Deep Reactive Ion Etching (DRIE). In particular an aluminum hard mask 600-800 nm thick has been evaporated and patterned by lift-off with the geometries previuosly described. Then, the etching process has been performed and at the end the aluminum hard mask has been stripped

chemically. Here we will report also the development of the "G" test structures aimed at evaluating the thermal conductance versus the Si resistivity. Required values of G are thus straightforward by shapes optimization work.
We have measured 3 devices with the same planar silicon geometry of the CryoAC DM and different silicon wafers. Silicon wafers differ for electrical resistivity, doping and thickness. Their resistivity were the following: 10 Ω·cm, 5 kΩ·cm and 10 kΩ·cm. The first two samples were p-doped with boron and they were 260 µm thick, whereas the third one was declared intrinsic by the producer and guaranted to a resistivity not less than 10 kΩ·cm, its thickness was 500 µm.

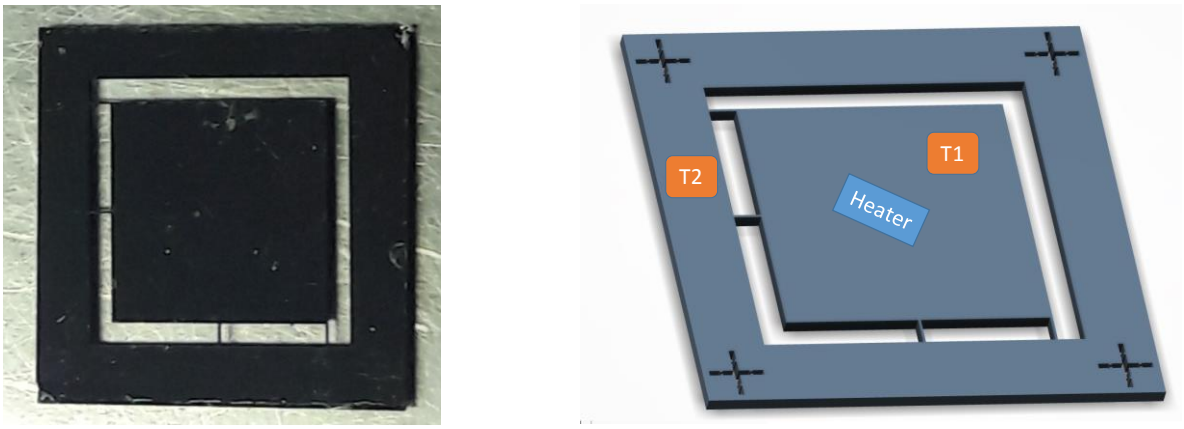

Fig. 3 - Picture of the DM-like thermal conductance measurement and sketch of the device with heater and thermistor locations.

Silicon wafers, have been etched using DRIE with Bosch process, as previously described, to fabricate a device with the same shape of the DM (Fig. 3). A detail of the silicon bridge is shown in the Fig. 1 where there is a scanning electron microscope image made after the silicon DRIE etching. The silicon bridges have been carefully observed with an optical profilometer for better investigating deviations from the ideal shape. We see a deviation of the lateral side of the bridges form the vertical plane: top-side width is 100 µm as expected, while the back-side is thinner, from 96 to 70 µm, these values are summarized in Table 1 for the different structures measured.
The thermal conductance measurement is made in the following way: the electrical power is released to the central part of the device so that the heat moves towards the rim, which is glued to the copper cold finger of the dilution fridge. When the heat flows through the silicon bridges a temperature difference occurs across them. This one is measured with two identical thermistors: one on the body of the freestanding silicon pixel, and the other on the rim. The heater is a small Ni-Cr meander resistor on 2x2 mm^2 chip. The thermistors are germanium sensors that have been glued with epoxy on suspended active area and on silicon rim, respectively. Thermometers and all electrical connection were glued with EE149 EPO-TEK®- silver resin paste whereas the heater is glued to the substrate with GE Varnish 7031. The electrical connections have been made with 12 µm diameter and 10 mm long Au:Be wire. A scheme of the device is also reported in Fig. 3.

#	Nominal Resistivity	Wafer Thickness (µm)	Beam Top width (µm)	Beam Bottom width (µm)	Beam Section ($µm^2$)	Beam length (µm)	*s/l* Geometrical Factor (µm)
1	10 Ω·cm	260	100	80	23400	1000	23.40
2	5 kΩ·cm	260	100	96	25480	1000	25.48
3	10 kΩ·cm	500	100	70	42500	1000	42.50

Table 1 - Silicon beams geometrical parameters of different samples.

3 "TEST STRUCTURES" TEST

In this section we discuss the test setup and experimental results of the produced test structures.

3.1 Theoretical introduction

In general, the heat power flowing in a thermal link is a function $W(T_1, T_2)$ of the two different temperatures:

$$P = W(T_1, T_2) \quad [1]$$

In our case, the two temperatures are the rim temperature T_1 and the suspended pixel temperature T_2 (see Fig. 3). We rewrite W as function of the average temperature $T = (T_1 + T_2)/2$ and the temperature difference between rim and suspended structure $\Delta T = T_2 - T_1$. From Eq. 1 at first order we obtain $P = W(T, \Delta T)$, by considering W at fixed T and expandind around $\Delta T = 0$:

$$P = W_T(\Delta T) = W_T(0) + \frac{dW_T(0)}{d\Delta T}\Delta \mathrm{T} \quad [2]$$

where $W_T(0) = 0$ for intrinsic physical reasons, and the coefficient of the linear term is by definition the conductance G:

$$G(T) = \frac{dW_T(0)}{d\Delta T} \quad [3]$$

thus, we can write at first order:

$$P = G(T)\Delta T \quad [4]$$

The Thermal conductance due to a solid beam can be written as follow:

$$G(T) = k(T)\frac{s}{l} \quad [5]$$

where *s* is the beam section, *l* is beam length and k is the material thermal conductivity. The thermal conductivity is the sum of two different contributions: the free charge (conduction electrons) and crystal lattice vibrations (phonons):

$$k = k_{el} + k_{ph} \quad [6]$$

At low temperature both components follow the same behavior of the specific heat: the electronic component has a linear dependence to the temperature, whereas the phonon component has a dependence to third power of the temperature.

3.2 Measurement setup

The measurement consists in injecting the power P in the heater and in reading out the resistance of the two thermometers, one on the suspended square and the second one on the rim. To perform the measurement of the effective dissipated power, we read both current and voltage drop on the heater with a four probes setup, whereas thermometers are measured with two probes applying a common constant voltage of about 0.5 mV and reading both the applied voltage and the currents with two pico-ammeters (see Fig. 4). We used the cryostat temperature control to stabilize the temperature and for each cryostat temperature T_0 we recorded the resistance of both Ge thermistors at different dissipated power P from 0 to ~ 1 μW. Thermometers calibration has been obtained considering germanium resistances without any power applied ($P = 0$), using the cryostat

calibrated thermometer as reference. The test setup is the same for all devices, and it is shown in Fig. 5.

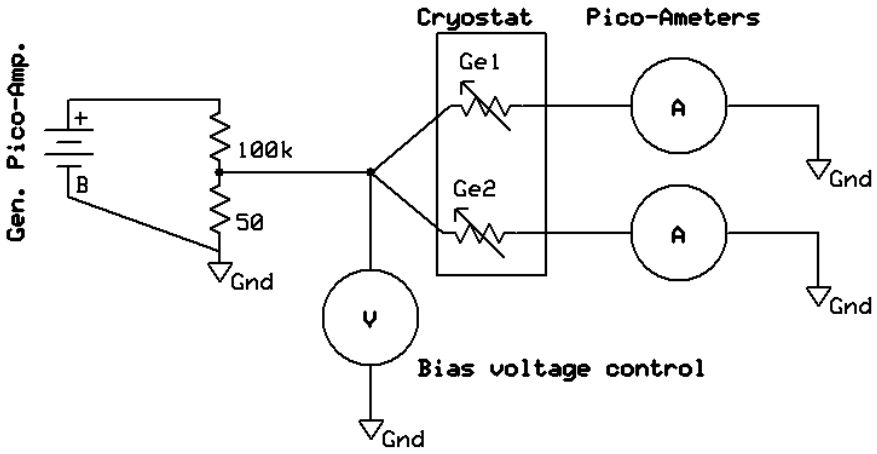

Fig. 4 - Thermometers readout scheme.

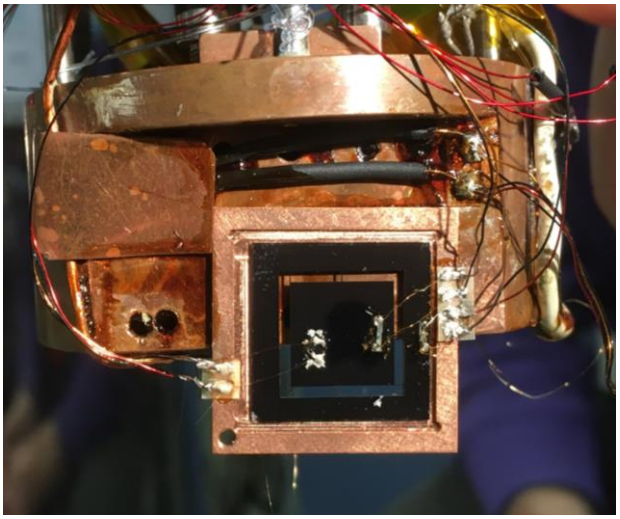

Fig. 5 - Pictures of test setup in the Kelvinox 25 at Phys. Dpt. Genova Univ.

3.3 Data analysis: thermometers calibration and conductance calculation

Two curves $R_1(P)$ and $R_2(P)$ were acquired at different cryostat temperature T_0. The values $R(P = 0)$ correspond to germanium thermistors calibrations $R(T)$. Anyway, to have a better evaluation we extrapolate the value at $P = 0$ with a linear fit, an example is reported in Fig. 6 - Left. Thus, the calibration data were fitted using the typical germanium thermistors resistance temperature expression:

$$R = R_0 e^{\sqrt{\frac{T_0}{T}}} \qquad [7]$$

Table 2 reports values for parameters R_0 and T_0 which we obtained for both thermometers in the different measurements. The expression has been inverted, obtaining the relation $T(R)$ for both germanium thermometers (see Fig. 6 - Right).
Therefore, for each average temperature we obtained the curve $P(\Delta T)$, power as function of temperature difference, and from its linear fit (in the ΔT range 0 – 50 mK) the thermal conductance. In Fig. 7 it is reported an example. We can observe the linear behavior at small temperature difference and the deviation from linearity at large difference.

#	Thermistor	R_0 (Ω)	T_0 (K)
1	Ge 1 (rim)	837.38	20.89
	Ge 2 (freestanding)	538.39	22.87
2	Ge 1 (rim)	28.82	6.94
	Ge 2 (freestanding)	9.08	10.49
3	Ge 1 (rim)	11.59	8.24
	Ge 2 (freestanding)	8.34	10.23

Table 2 - Calibration parameters values for the different samples.

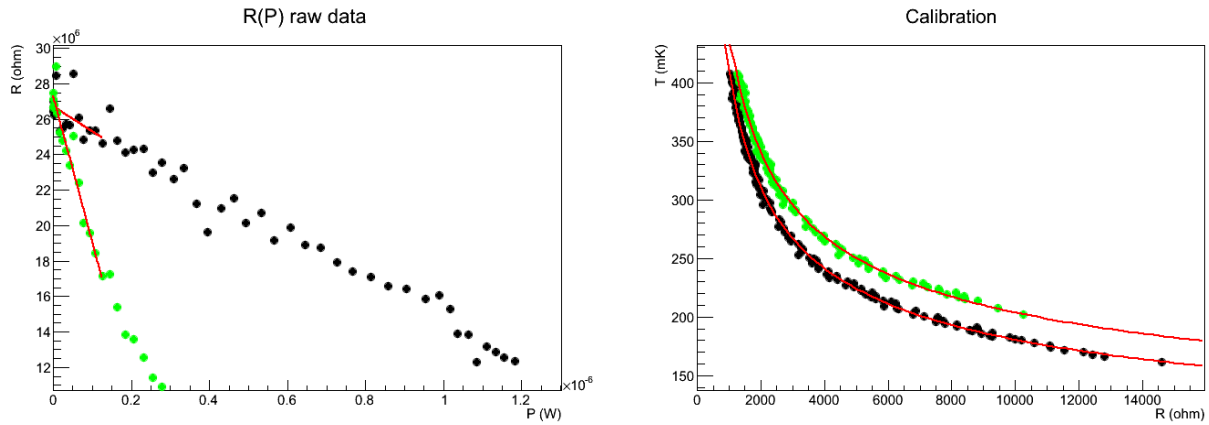

Fig. 6 - Left - Example of R(P=0) extrapolation. - Right - Calibration fit. black is Ge1 (rim) and green is Ge2 (freestanding).

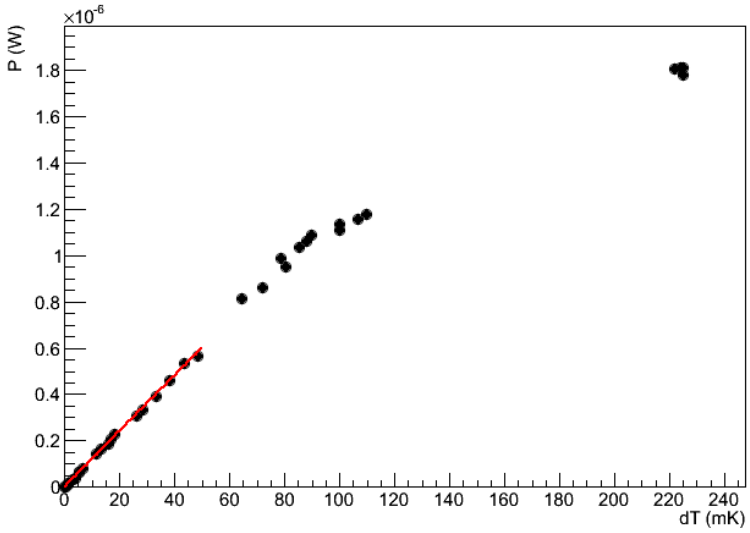

Fig. 7 - Plot of P(ΔT) curve and linar fit at ~ 257 mK of rim for test #1.

3.4 Results

Fig. 8 shows the plots of G(T) curves for the different samples, as direct result from the measurements. The red line is a fit and highlights a trend with temperature which is a combination of a linear and a cubic term:

$$G(T) \propto aT + bT^3 \quad [8]$$

Values of thermal conductivity for each sample have been obtained normalizing both the "G" data and fitting parameters by the related geometrical factor (Table 1). Fig. 9 shows the thermal conductivity for all different tested silicon samples, and Table 3 reports the related fit parameters normalized using geometrical factor available in Table 1.
Table 4 reports the expected DM thermal conductance calculated using fit parameters of Table 3 and considering 4 silicon beams, each one with a section of 100x500 μm^2 and a length of 1 mm (geometry factor 50 μm).

#	Nominal Resistivity	a $(\frac{\boldsymbol{W}}{\boldsymbol{K^2 \cdot m}}) \cdot \boldsymbol{10^{-3}}$	b $(\frac{\boldsymbol{W}}{\boldsymbol{K^4 \cdot m}})$	K @ 50 mK $(\frac{\boldsymbol{mW}}{\boldsymbol{K \cdot m}})$
1	10 Ω·cm	391.5 ± 0.3	1.483 ± 0.003	19.76 ± 0.02
2	5 kΩ·cm	52.3 ± 0.9	2.095 ± 0.015	2.88 ± 0.05
3	10 kΩ·cm	42.7 ± 0.4	0.829 ± 0.004	2.24 ± 0.02

Table 3 - Normalized fit parameters.

#	Nominal Resistivity	G @ 50 mK 50 μm s/l $(\boldsymbol{\mu W/K})$
1	10 Ω·cm	3.953 ± 0.002
2	5 kΩ·cm	0.576 ± 0.005
3	10 kΩ·cm	0.448 ± 0.003

Table 4 – Extrapolated DM thermal conductance at 50 mK.

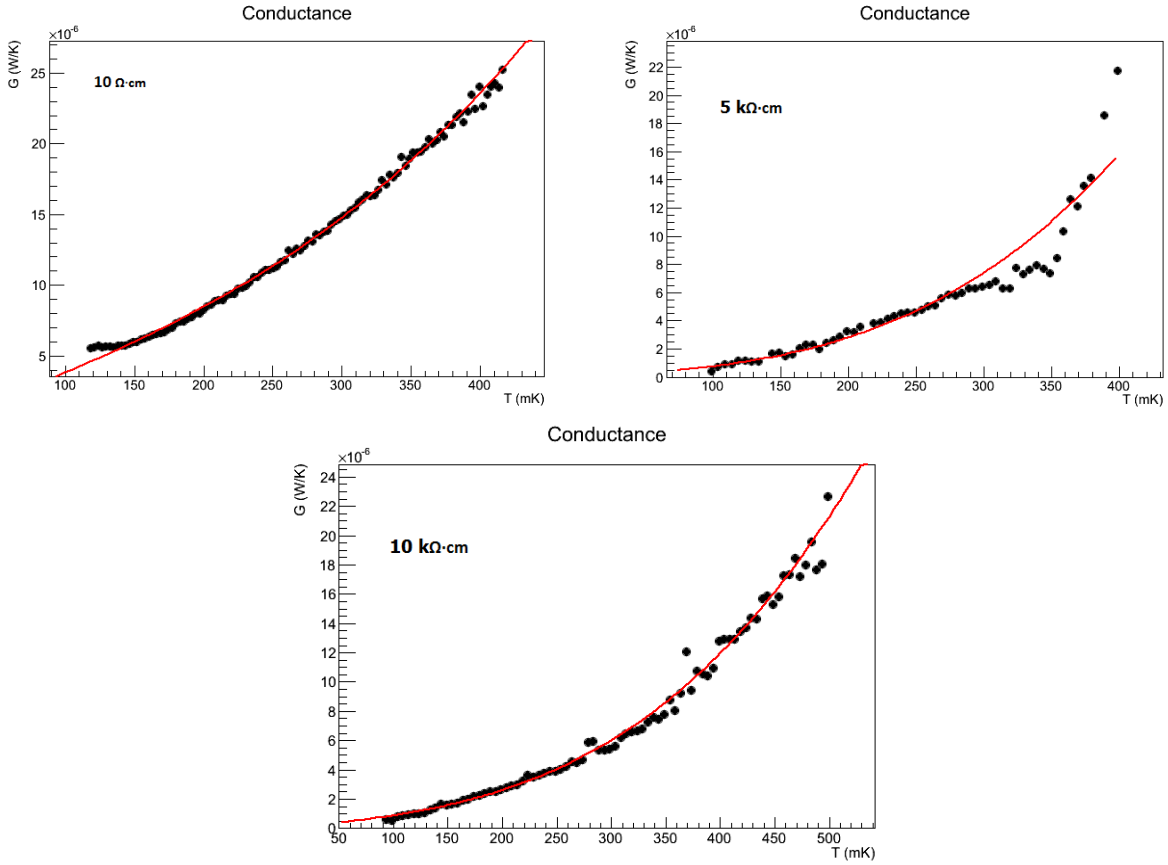

Fig. 8 - Plot of G(T) curve for DM-like test structures.

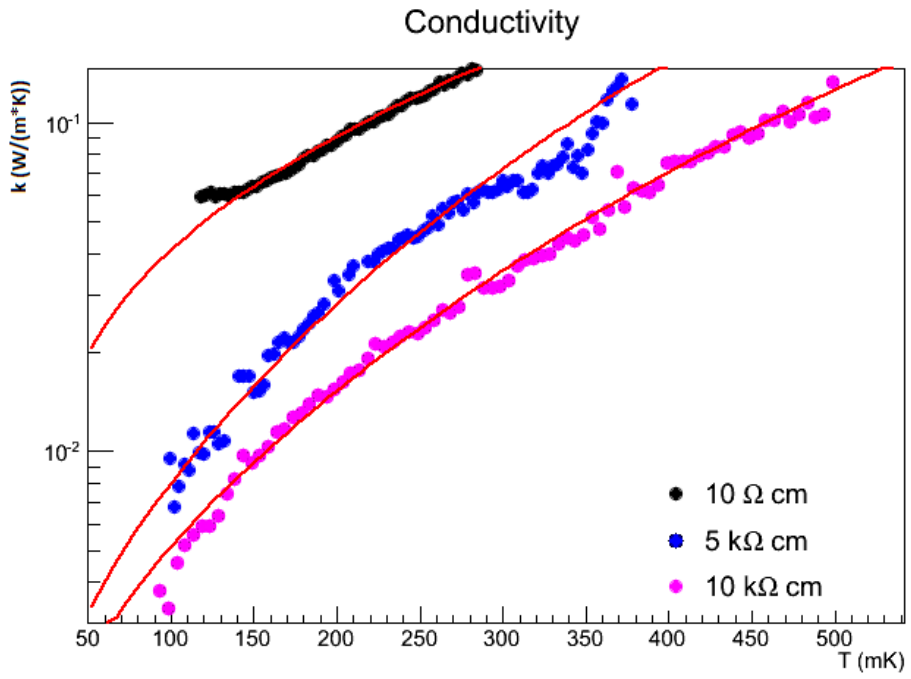

Fig. 9 - Thermal conductivity of different silicon wafers tested.

In our CryoAC concept design we have calculated a thermal conductance of $2 \cdot 10^{-8}$ W/K at 50mK, about a factor 20 below the lowest measured with the test structures (~$4 \cdot 10^{-7}$ W/K at 50mK, corresponding to a Si resistivity of 10 kΩ·cm). This is due to the fact that we had not taken into account the electron linear contribution, which the test structures measurements have revealed to be predominant for the tested Si samples. However, this electron component also affects the specific heat of the absorber, thus the thermal time constant of the detector and the energy resolution. All these parameters affect the Dead Time (DT < 2% TBC on the full CryoAC array is the present requirement). We have now re-evaluated the expected thermal capacity of the DM (83 pJ/K at 100 mK, instead our previous evaluation of 40 pJ/K) and, taking into account the present G measurement (assuming a 10 kΩ·cm Si resistivity as baseline), we obtain a faster thermal time constant with respect to our previous one (about 0.2 ms with respect to~2 ms), thus providing in principle a lower DT. At present, the increased heat capacity provides a thermal energy resolution at 100 mK of about 0.6 keV@15 keV.

3.5 SIMS analysis

We have investigated the possibility that the previous measurements were compromised from a low quality of the Silicon samples adopted. For this reason we have commissioned to FBK in Trento (Italy) bulk and surface analysis of impurities by means of SIMS and XRF.
The impurity analysis results show that only in the lowest resistivity sample is found an excess of Li and B ions. The measurement don't show any excess of the monitored ions respect to instrument sensitivity for the high resistance samples. Surface analysis shows contamination of Zn and Fe, excluding possible heavy doping.

Codice FBK	Analisi SIMS (atomi/cm^3)
L328	Li = 2 E12 B = 2.3 E15 N = 6.5 E16 Al = 1.3 E14 P = 1.4 E15 Ca = 1.9E14 Zn = 3.0E16
L329	Li = 7 E11 B = 7.0 E14 N = 6.4 E16 Al = 1.5 E14 P = 7 E14 Ca = 1.7E14 Zn = 2.4E16
L330	Li = 9 E11 B = 8.2 E14 N = 6.4 E16 Al = 1.3 E14 P = 1.4 E15 Ca = 2.0E14 Zn = 2.6E16

*SIMS analysis of the sample with nominal resistivity 10 Ohm*cm, 5kOhm*cm, 10KOhm*cm (L328, L329, L330 respectively): only Li and B exceed the sensitivity of the measurement in the first sample.*

4 THE AC-S9 TEST RESULTS

A testing activity on AC-S9 based on Si chip having resistivity greater than 10 kOhm*cm has been performed [RD2]. As shown, this detector has higher thermal capacitance than the expected DM since it is not etched (absorber not suspended).
It has been biased at the thermal bath temperature of 50 mK as required for the Athena X-IFU, and back illuminated by ^{55}Fe (6 keV line).

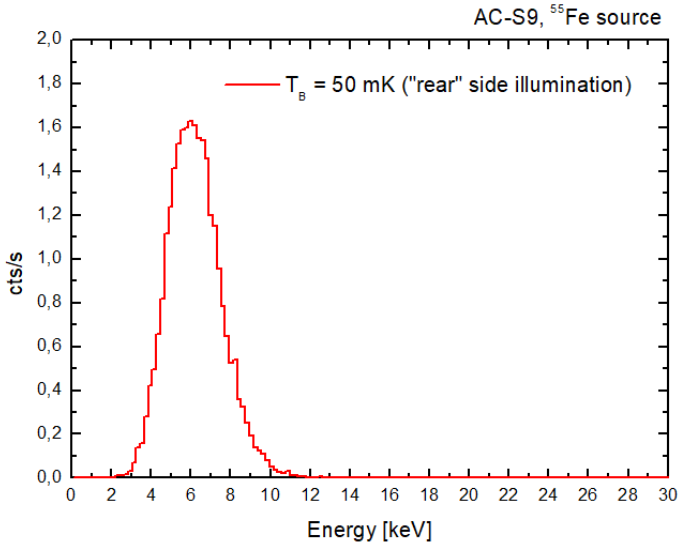

Fig. 11 – Energy spectra acquired back illuminating the AC-S9 detector by means of a ^{55}Fe source (6 keV photons).

The result shown is quite (~3 keV@6keV) promising in the context of a consolidation-study for a spectroscopic CryoAC. Our feasibility study report few keV@20keV to perform science analysis by the CryoAC.

5 CONCLUSION

In this TN we have reported the outcome related to the test structures activity and Si chip chemical composition. We have seen that the dopant contribution in Si, i.e., the Si resistivity, has an impact on the thermal conductivity thus affecting the detector time constant and the energy resolution.
We have developed and tested a sample (AC-S9) having resistivity greater than 10 kOhm*cm. The results are promising, and they show that this kind of detector, though designed for particle rejection, has some interesting spectral capability that could be probed towards a scientific use of this detector.