



SRON-AHEAD-RP-2018-002

# Summary of FDM test setups at SRON

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|---|---|
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At SRON 6 setups for testing of the detector and read-out chain are available and these are described in the attached document (FDM setups, 22 May 2018)

SRON
Netherlands Institute for Space Research

# Summary of FDM setups at SRON

## Introduction

We have 6 FDM setups currently operational at SRON. There are 4 similar experimental FDM systems, namely *XFDM*, *FDM_probe*, *FDM_large and EFDM* that each can read out 18 TESes (fig. 1).

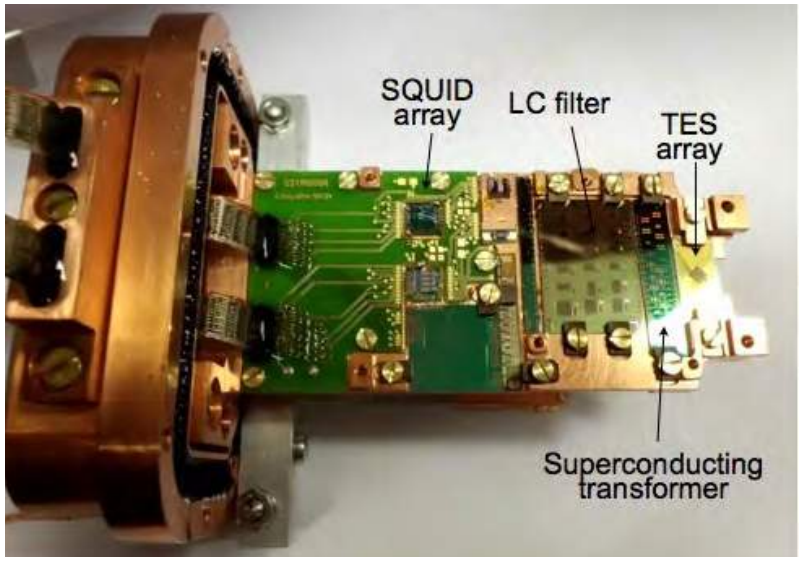



Fig. 1. A picture of the *XFDM* setup with 18-pixel FDM readout system.

There are also two identical 40-pixel readout systems, namely *40-pixel-A* and *40-pixel-B*, which can accommodate large (i.e. 1k-pixel) TES arrays (fig. 2).

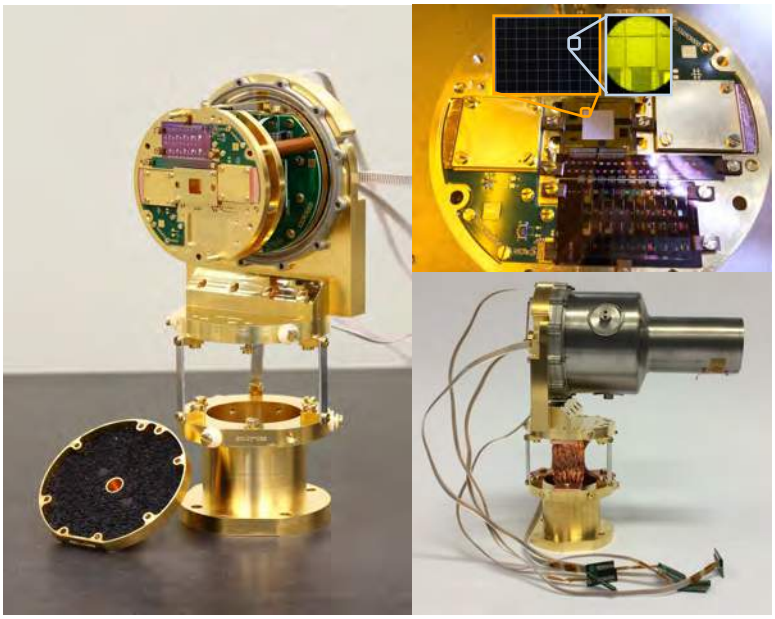


Fig. 2. Pictures of the 40-pixel-A setup that can accommodate 1k-pixel TES array and readout capability of 40 pixels at the same time.

## Readout Circuit

In principle all readout circuits are very similar to what is shown in fig. 3. The AC bias is provided by the DEMUX digital electronics at the bias lines that go through the Front-End-Electronics (FEE), where the series bias resistance is set and continues to the cold part. There we typically have a shunt resistor, followed by a capacitive voltage divider and the LC resonators. Each resonator is in series with one TES that defines its frequency channel. If necessary, a transformer chip is used in between to match the impedance of the TESes to the readout circuit. All signals are then come together at the summing point and read out by a FE-SQUID and amplified by an AMP-SQUID.

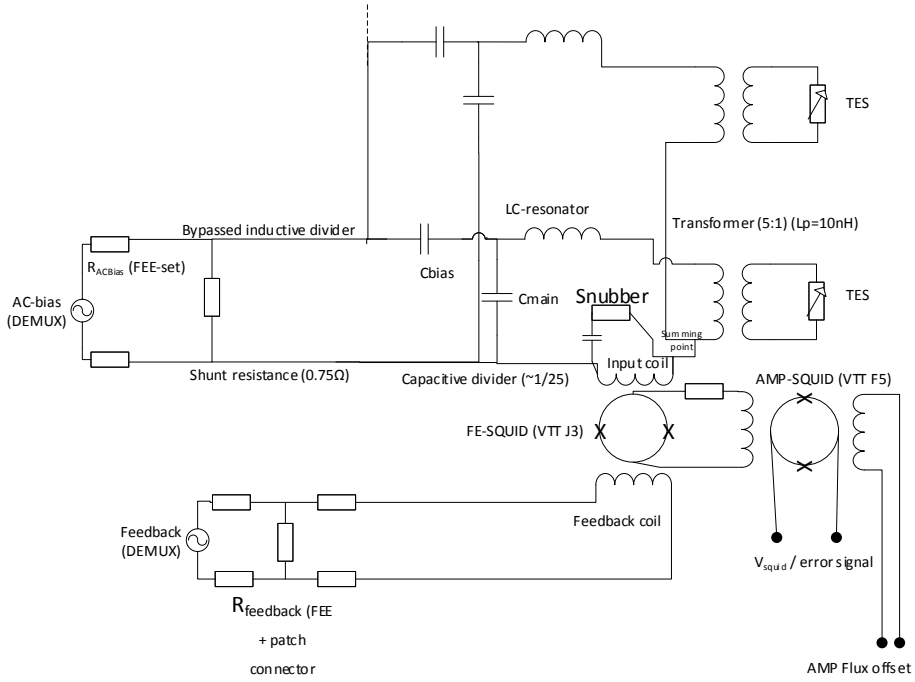



Fig. 3. Schematic picture of the bias circuit of the FDM setups

The signal is then further amplified by an LNA and demodulated by the DEMUX, which also provides the feedback signal to lock the SQUID (fig. 4).

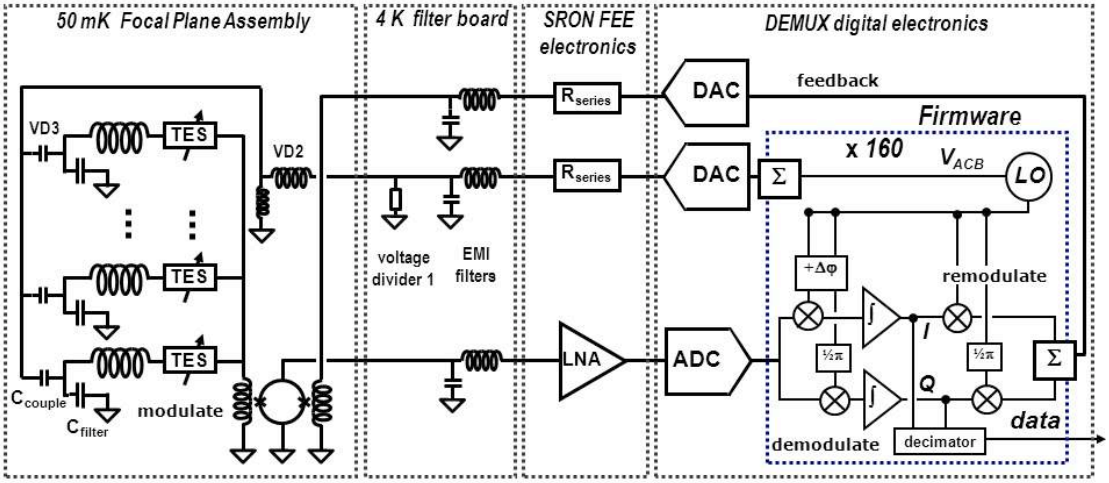



Fig. 4. Schematic picture FDM readout system including the baseband feedback (BBFB).

There are small differences between the setups that are summarized in Table 1. XFDM and FDM_probe setups are currently used to demonstrate the ultimate performance of the X-IFU TES detectors and the multiplexing. FDM large is dedicated to SRON detector development. EFDM setup is the Engineering channel to test different components in the readout change independently but is fully capable of characterizing detectors too. 40-pixel-A setup is assigned to demonstrate large array readout capabilities. 40-pixel-B is now used for VTT SQUID tests in cryogenic temperatures but later this will be used to test the X-IFU DM arrays and after that SRON 1k-pixel arrays.

Table 1. Summary of the parameters in experimental FDM setups.

| Parameter | XFDM | FDM_probe | FDM_large |
|---|---|---|---|
| Shunt | 0.75 Ω | 0.75 Ω | 0.1 Ω |
| Capacitor divider | 01:25 | 01:25 | 01:25 |
| LC resonators | LC18-2 7a (18-pixel; 2uH) | LC17-6 Chip 2 (18-pixel; 2µH) | 17-12 chip 3 (18-pixel; 1uH) |
| Transformer | SC11-1 chip 8a (1:3 Lp=32nH) | SC11-1 7b (1:2 Lp=48nH) | SC07-2 chip 4a (interconnect) |
| FE SQUID | VTT J3 (Ret N) | VTT J3 (Ret M) | VTT J3 (Ret P wafer #28) |
| AMP SQUID | VTT F5 (CGG#5) | VTT F5 (EIG#1) | VTT F5 (IGG#3) on coldfinger |
| Snubber at summing opint | 5 Ω – 1 nF | 5 Ω – 1 nF | 5 Ω – 1 nF |
| Best Xray results | 1.8 eV | 1.9 eV | 3.9 eV |

| Parameter | 40-pixel-A | 40-pixel-B | EFDM |
|---|---|---|---|
| Shunt | 1.0 Ω | 0.27 Ω | 1.0 Ω |
| Capacitor divider | 01:25 | 01:25 | 01:25 |
| LC resonators | LC17-1 chip 1b (40-pixel; 2uH) | LC17-1 chip 1a (40-pixel; 2uH) | LC18-x chip 3 (18-pixel; 1uH) |
| Transformer | SC10-3 chip 4a (1:8 Lp=10.3nH) | none | none |
| FE SQUID | VTT J3 retO | Varies (VTT K1) | VTT J3 (ret V wafer#28) |
| AMP SQUID | VTT F5 IEG#9 | Varies | VTT F5 (ret.1 'c' or p) |
| Snubber at summing opint | 5 Ω – 1 nF//6.8 pF | no | 5 Ω – 1 nF |
| Best Xray results | 3.6 eV | No array | No array |

For each of these setups there are log files for each run that the all the changes in that run is documented. Appendix 1-5 are examples of such log files.

## Appendix 1
## XFDM setup overview

# Wirebonding overview: XFDM setup Run 71

**Prepared by: Kevin Ravensberg**

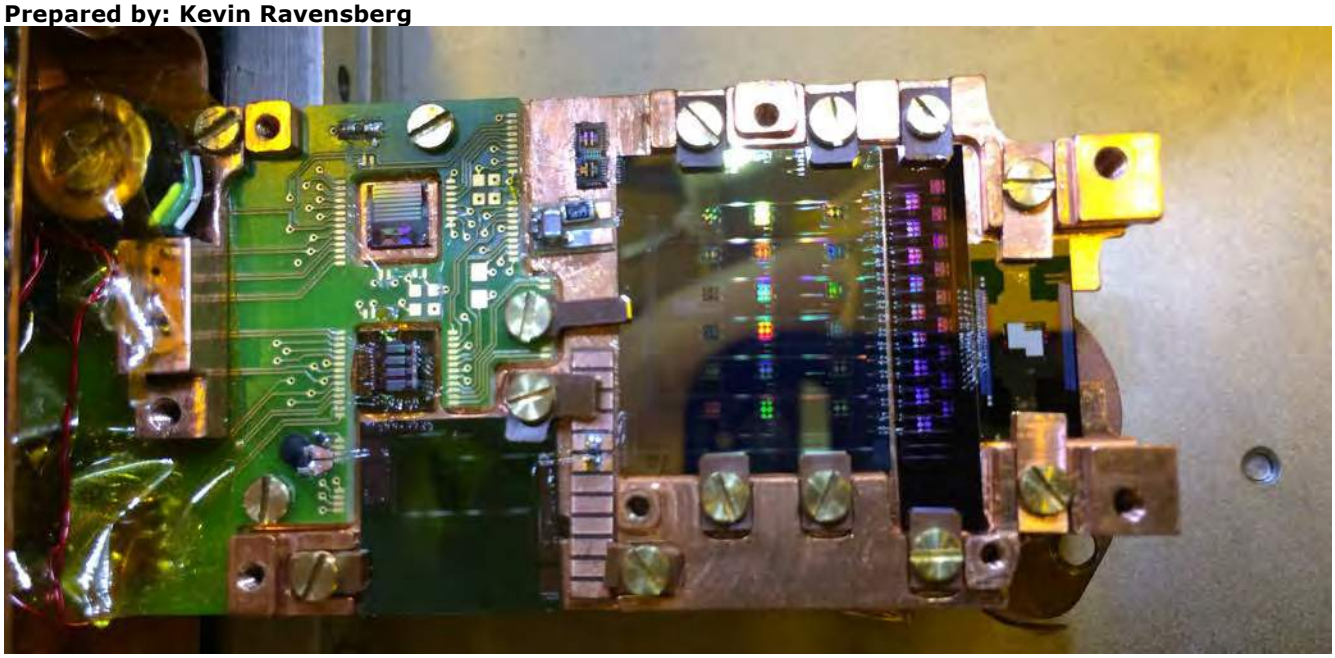


**Figure 1. XFDM setup with uniform A6 GSFC TES array, as of LC run 71.**

***Table of contents:***

# 1 Modification overview:

In run 71 the transformer chip was replaced with a 1:3 ratio version from the same wafer, also all 18 channels have a TES connected to go for 18-MUX factor measurements.
In run 71 the TES array was replaced with the uniform pixel size GSFC A6 – array, previously the A4 uniform array was used. New gold wire bonds have been placed to thermalize the new TES array as good as possible.
In run 66 we added the ''snubber'' circuit to the LC-filter summing point. This is a lowpass RC-filter consisting of 5 Ohm resistance with 1nH capacitance in series, the circuit itself is a connected parallel to the Input SQUID input coil, damping all high frequency oscillations that pass through the summing point line of the LC filter chip.

## 1.1 Au-wirebonding

The J3 (RetR VTT) 6-SQUID array SQUID has an added Au wire bond parallel to the Al wire for better thermalization of the SQUID. Also the AMP-SQUID already had two Au thermalization wire bonds between the SQUID bias pads and PCB (from Run 52). To improve the thermalization of the ACbias shunt resistance, here one Au wire bonds is connected to the large interconnect chip.

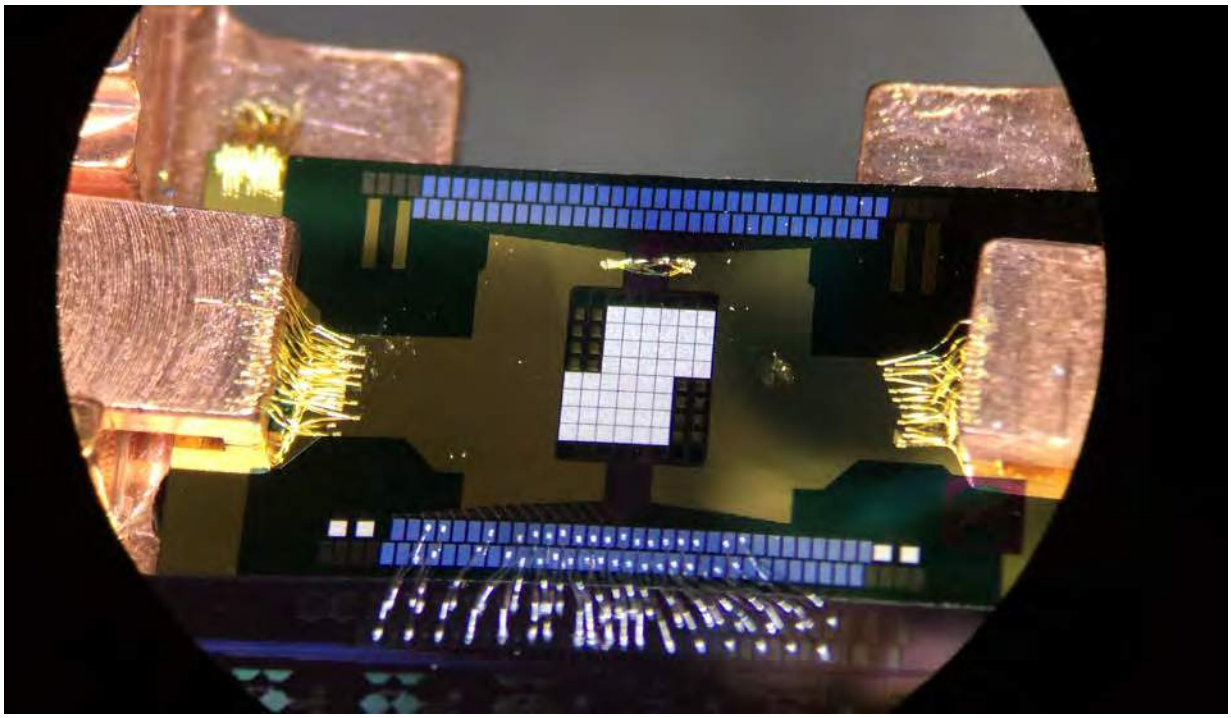


**Figure 2. TES array after placing thermal Au-wire bonds from clamps and bracket.**

20+ wire bonds per side should keep the array as close to the bath temperature as possible, we did notice a significant high amount of thick bump bonds from previous experiment at NASA Goddard on other chips.

### 1.2 Replaced AC-bias shunt resistance

With the updated LC-filter we needed a 0.75 Ohm shunt resistance value, instead of the 0.1 Ohm used until Run 62.

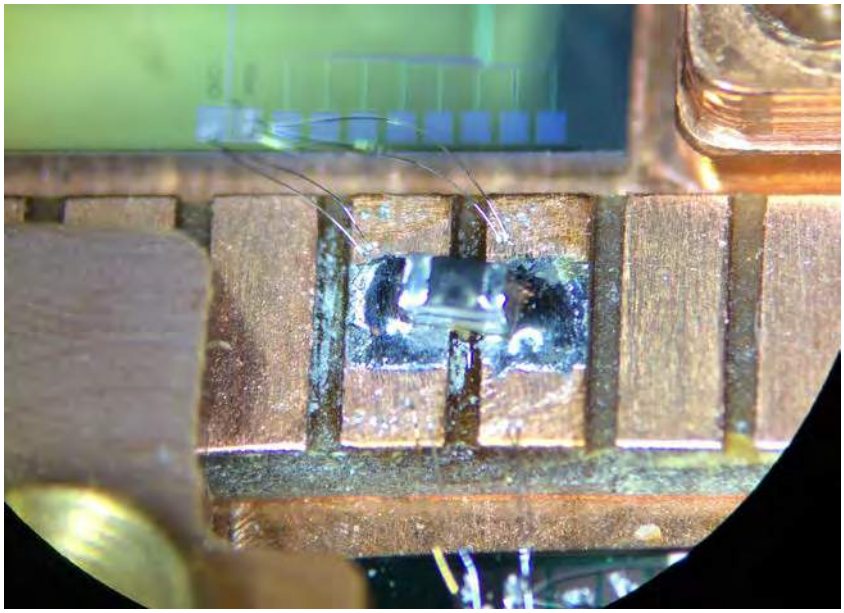


**Figure 3. Stacked 1.5 Ohm SMD resistors on the copper PCB as new AC-bias shunt resistance.**

### 1.3 Kevlar suspension - modified in Run 61

From Run 61 on the Kevlar suspension was modified to no longer damage the fragile wire by clamping the screw. Now there is a washer with a cylinder inside that keeps the wire from touching the brass screw.
A test was done to try at what tension on the screw the Kevlar wire gets damaged, and with maximum power it did not break.

**Figure 4. XFDM setup with modified**

Cu-plate thickness: **11mm**
Cu-plate diameter: **110mm**
Kevlar wire section length (1/6$^{th}$ of total): **124mm**

### 1.4 Uniform A6 (100um) TES array (Goddard) Run 71

In Run 71 we placed TES array A6 from GSFC on the setup. There are various defects on corner pixels, which have not been connected this run.

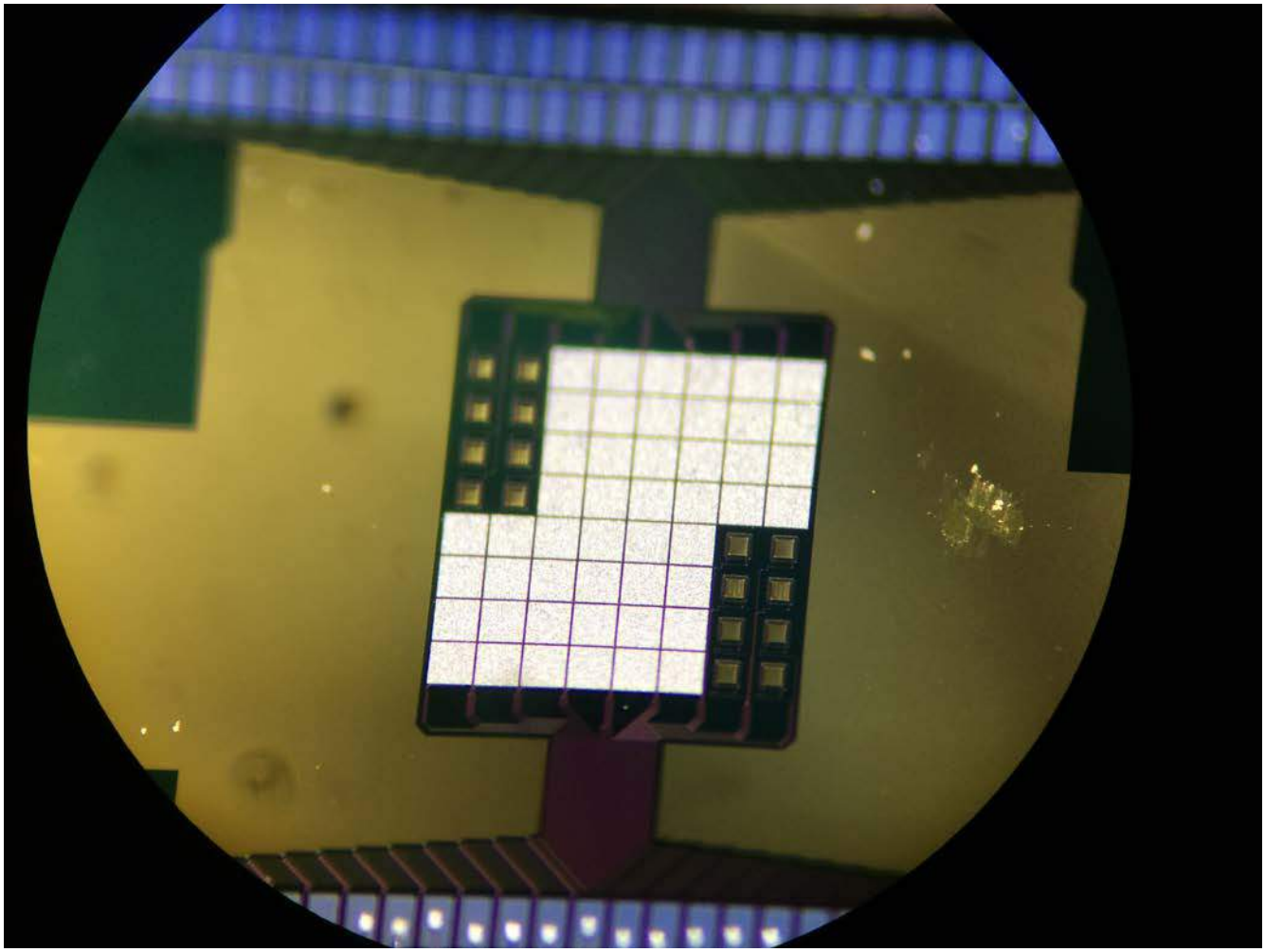


**Figure 5. A6 TES array from GSFC.**

### 1.5 LC-filter chip - 2uH version (LC18-2 7a with 12/18 resonators connected)

A new 2uH coil LC-filter is used with a on chip summing point at the SQUID side. The bias capacitor division C/Cbias=25 instead of 10 from the previous design, so the shunt resistance has been increased to compensate.

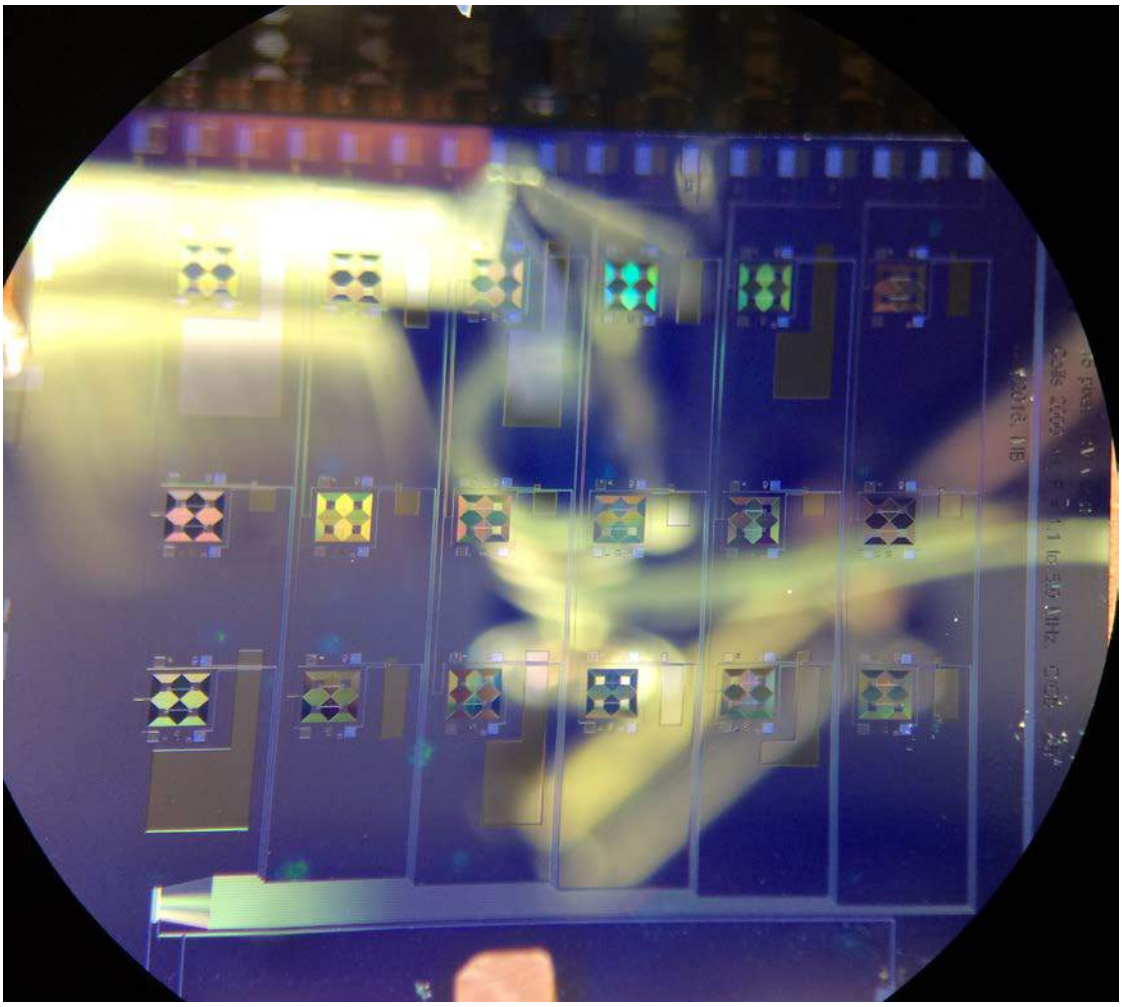


**Figure 6. LC-filter chip LC-18-2 Chip 7A**

### 1.6 Trafo chip 1:3 ratio (wafer SC11-1 chip 8a) introduced run 71

An all 1:3 trafo chip is used on the setup, with estimated coupling factor of the order of 0.9.
Primary coil has an inductance designed to 32 nH.
All transformers are expected to work well from room temperature measurements.

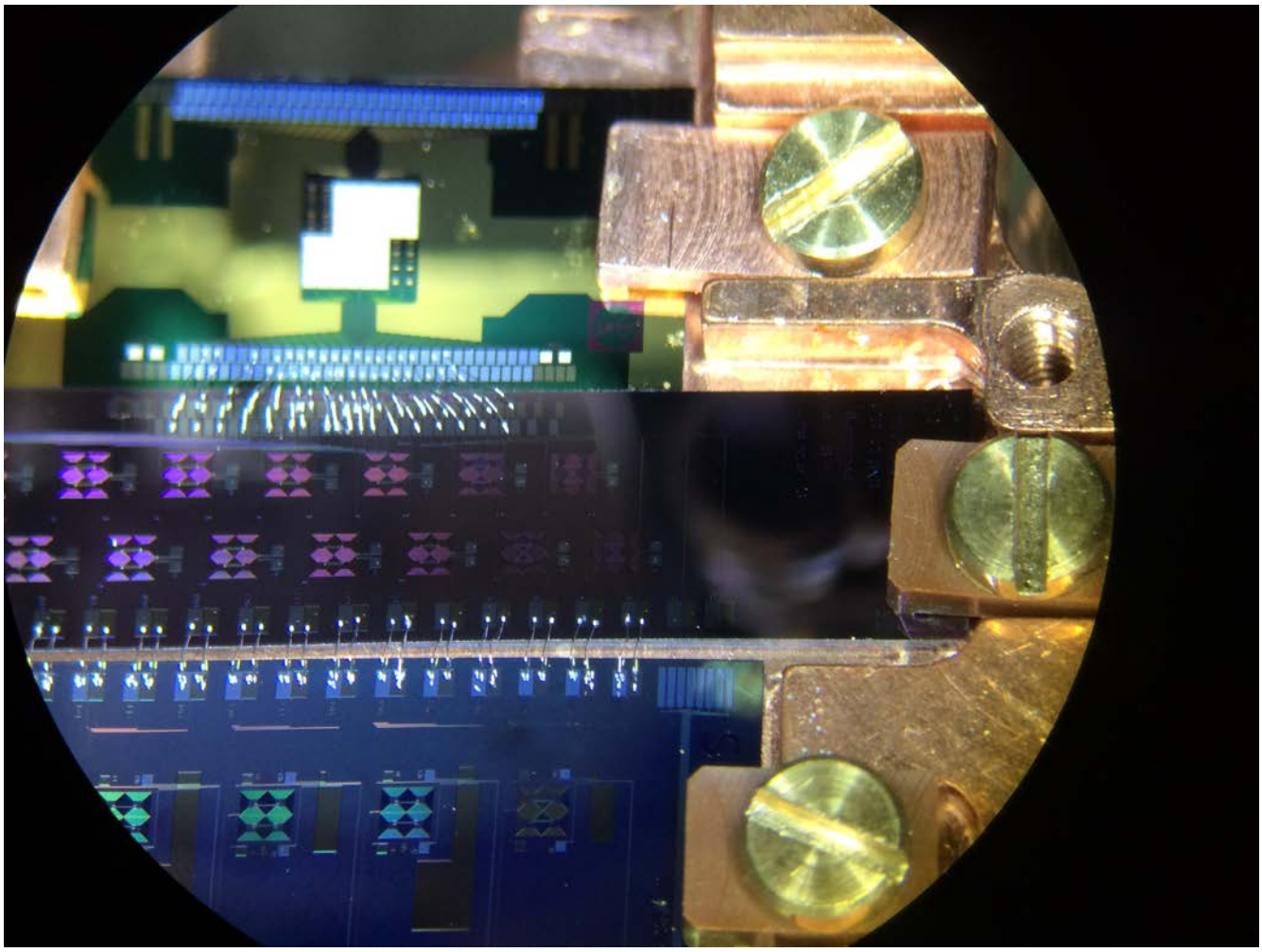


**Figure 7. SC11-1 chip 8a, all 1:3 ratio trafo chip.**

### 1.7 Snubber circuit

To damp the possibly troubling high frequency oscillations (100MHz+) between the Input SQUID and LC-filter chip, a lowpass RC-filter has been added to the setup in Run 66. An identical circuit was tested in the previous run on the Probe, where it improved the SQUID stability (cleaner V/Phi response and no/few oscillating noise peaks).

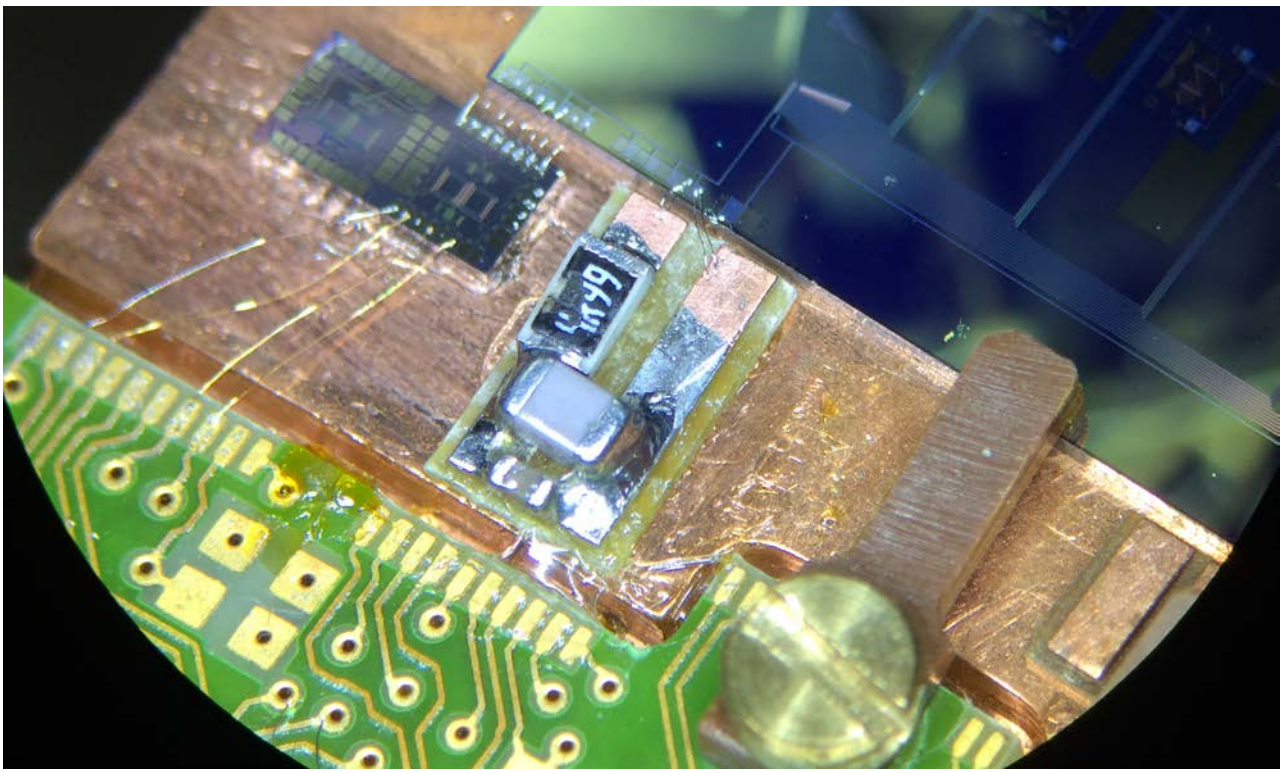


**Figure 8. Snubber circuit as used from LC run 66 in the XFDM setup.**

## 2 Wirebonding overview

A set of 18 TES pixels have been connected between 1.1MHz - 5MHz, with a representative frequency spacing of ~100kHz between most of the LC filter channels. This array only has 100um size TES's with absorbers. We have 18 pixels available for MUX mode experiments.

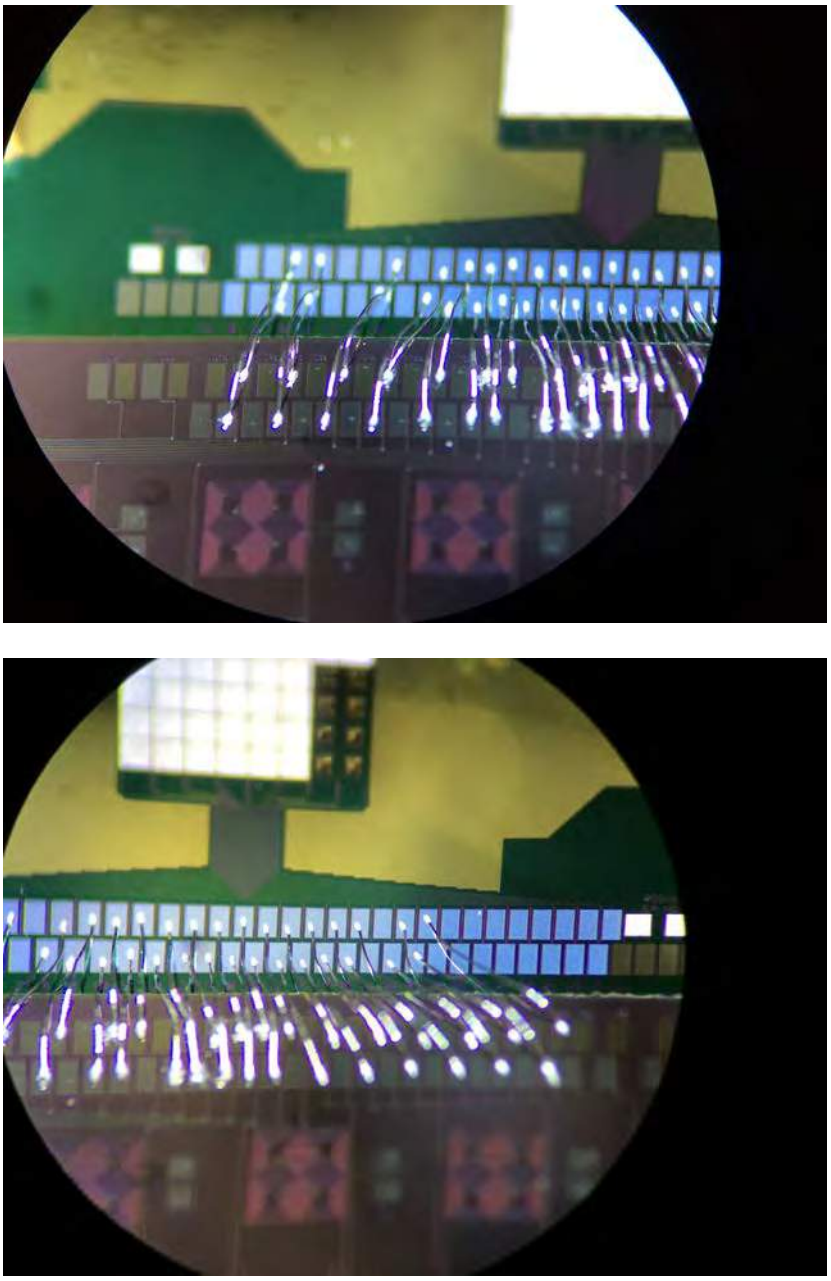


**Figure 9. Close up image of trafo - TES pad wire bonds, as of 13-4-2018.**

### 2.1 Overview of setup

The 2uH coil LC filter chip has been connected again, chip **LC 18-2** chip **7a rev 14.0**. Together with a 1:3 ratio transformer interconnect chip (**SC11-1 8a**).

**Table 1. Wirebonding overview of TES devices, 23-2-2018.**

| *LC-nr* | *Frequency (kHz)* | *Trafo nr* | *Trafo ratio* | *TES nr* | *Est. Frequency k=0.8 (kHz)* |
|---|---|---|---|---|---|
| 1 | 1100 | 3 | 3 | **6 (stripes)** | **1091,14** |
| 2 | 1200 | 1 | 3 | **2 (stripes)** | **1190,34** |
| 3 | 1300 | 9 | 3 | **13** | **1289,53** |
| 4 | 1400 | 7 | 3 | **11** | **1388,73** |
| 5 | 1500 | 15 | 3 | **19** | **1487,92** |
| 6 | 2000 | 13 | 3 | **17 (stripes)** | **1983,90** |
| 7 | 2700 | 6 | 3 | **10 (stripes)** | **2678,26** |
| 8 | 2800 | 4 | 3 | **8** | **2777,46** |
| 9 | 2900 | 12 | 3 | **16** | **2876,65** |
| 10 | 3000 | 10 | 3 | **14 (stripes)** | **2975,84** |
| 11 | 3100 | 18 | 3 | **23** | **3075,04** |
| 12 | 3200 | 16 | 3 | **20** | **3174,23** |
| 13 | 4000 | 11 | 3 | **15** | **3967,79** |
| 14 | 4600 | 5 | 3 | **9** | **4562,96** |
| 15 | 4700 | 17 | 3 | **22** | **4662,16** |
| 16 | 4800 | 8 | 3 | **12** | **4761,35** |
| 17 | 4900 | 14 | 3 | **18** | **4860,55** |
| 18 | 5000 | 2 | 3 | **3** | **4959,74** |

The TES's are from the A6 (Uniform 100um TES design) array, which was not tested at GSFC before.

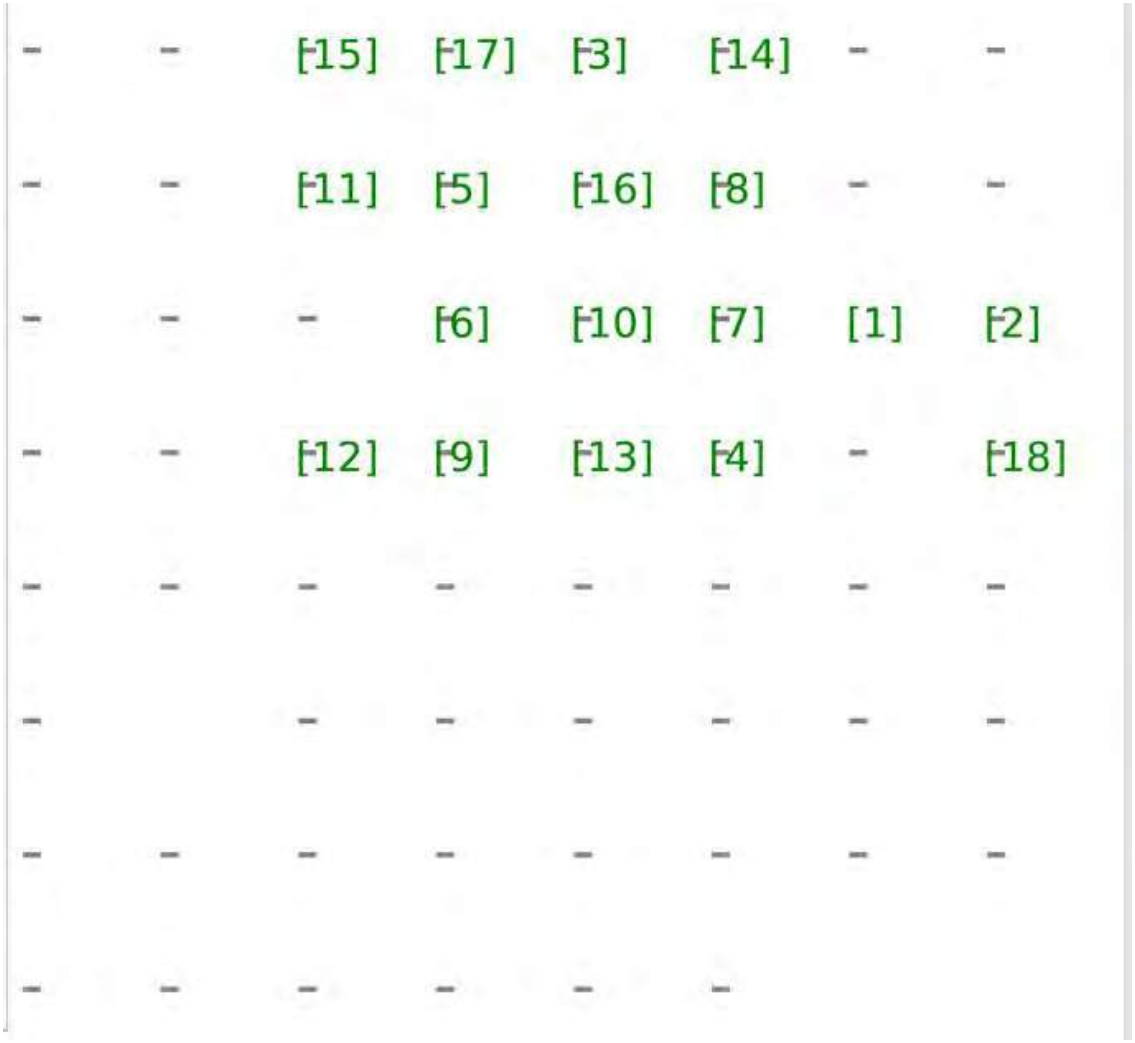



**Figure 10. LC-filter # vs location of connected TES on array (quadr=1, but array was rotated).**

TES's which have been identified as possibly broken: 0 26 31
On the other side: 10? or 21?
All these have been avoided, except for TES #10, but this one should be on the other quadrant (might be mistaken with rotation/mirroring of microscope image!). See pictures below for the microscope image.

## 3 Schematic overview:

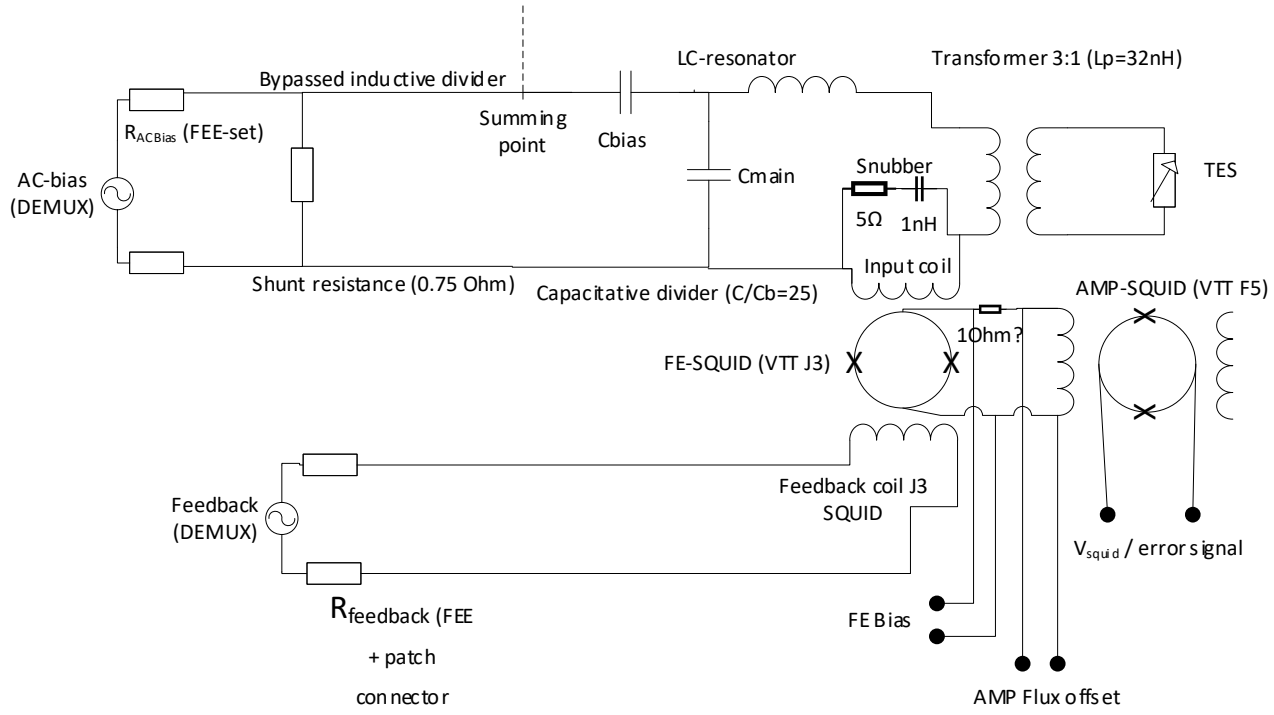



**Figure 11. Circuit diagram of LC resonators / TES between AC-bias and FE-SQUID (example for single resonator).**

AMP SQUID feedback applied via Input coil! This F5 SQUID was used in the XFDM-Probe before, showing no/little distortion in the V-Phi curve.

The G1 SQUID has been replaced by a J3 array-SQUID (6), which should show a decreased change in noise as a function of flux set-point.

Location of Snubber added to simplified diagram above, mounted in LC run 66.

## 4 Pictures

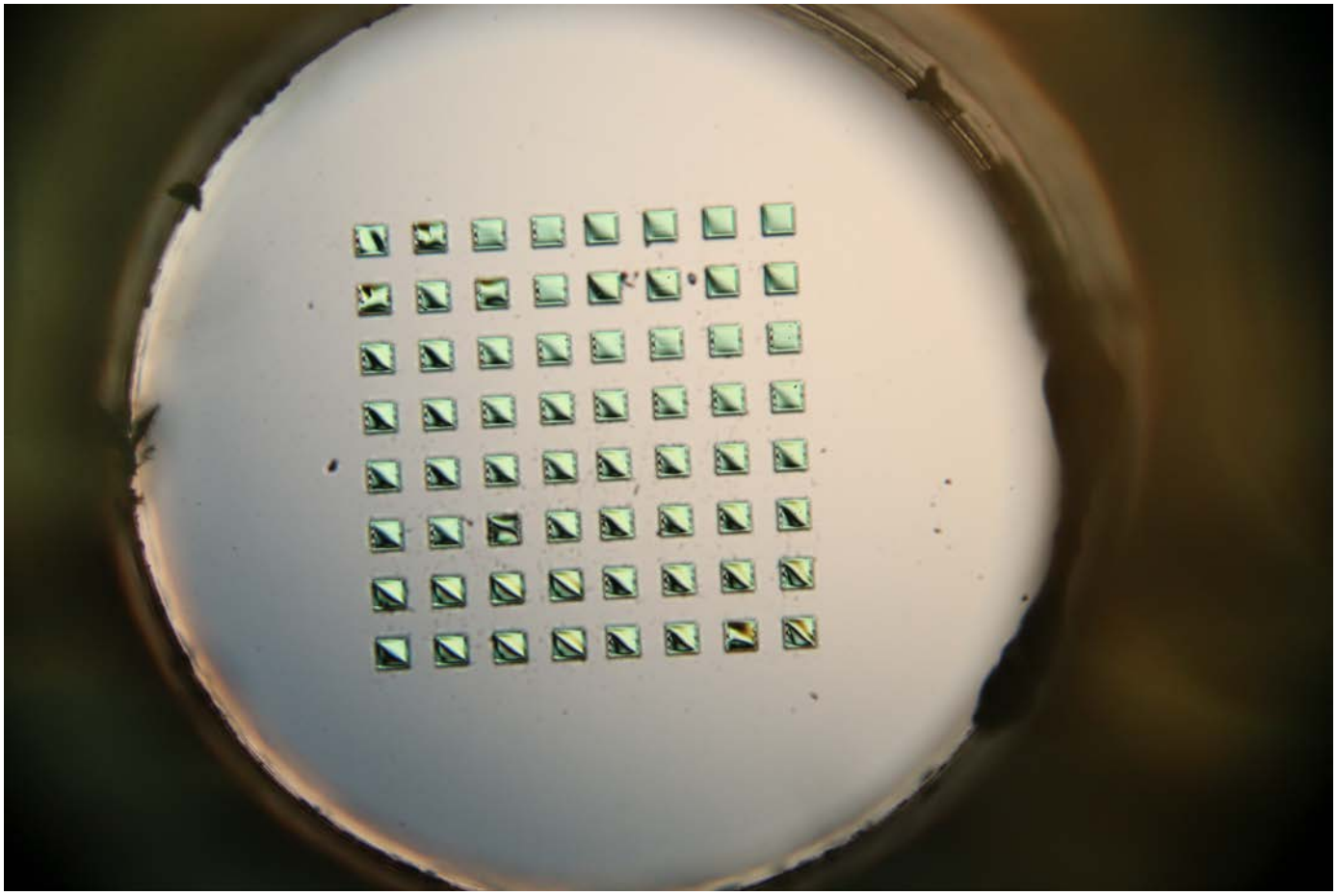


**Figure 12. GSFC A6 array as it arrived at SRON, before mounting in LC run 71 (8-3-2017).**

Several bent and a few broken membranes are visible with polarized light microscopy.

**Figure 13. Kevlar suspension, with copper thermalization straps to the 50mK plate.**

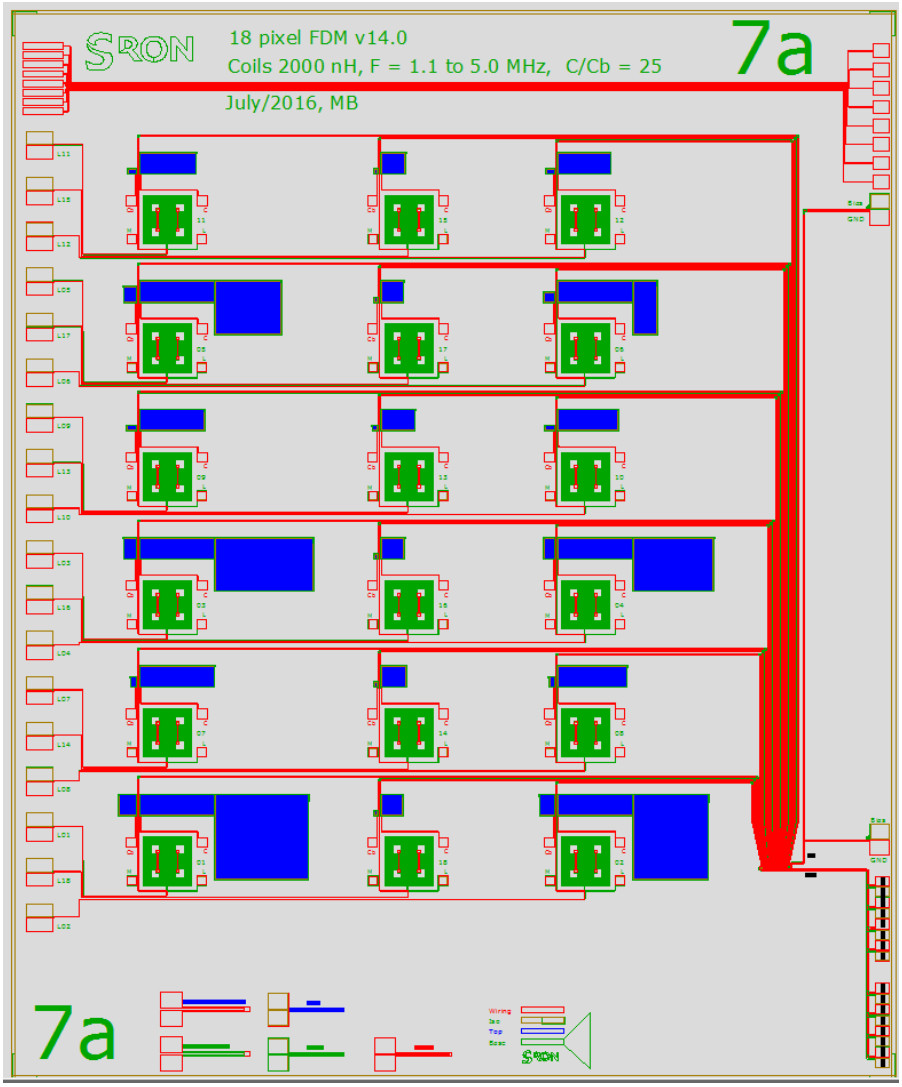



**Figure 14. LC-filter design v14.0 with integrated summing point.**

## Appendix 2
## FDM_probe setup overview

**Experimental setup overview: X-FDM_Probe Run 71**

**Prepared by: LG, Kevin Ravensberg**

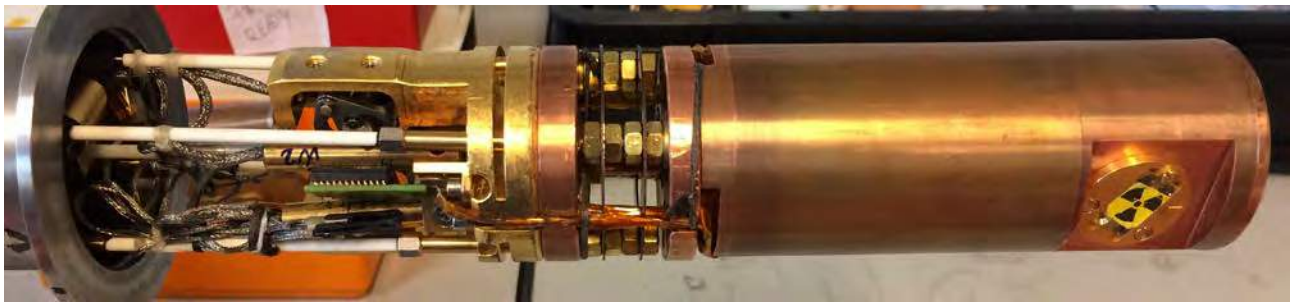


**Figure 1. Setup with VTT J3 (Ret M) FE-SQUID and EIG#1 F5 AMP-SQUID, TES array A5, picture from before Run 71.**

***Table of contents:***

## 1 Modification overview:

This run GSFC **A5** TES array (mixed size with/without absorbers) is mounted in combination with a **LC17-6 chip 2** 2uH LC filter chip (not changed) and the room temperature tested 1:2 **transformer chip SC11-1 chip 7b with Lp=48nH**. The summing point chip has been removed and is integrated now in the new LC filter chip. SQUIDs have not changed, F5 EIG#1 and J3 RetM. The J3 SQUID input coil has been wire-bonded again to the new LC-filter chip, only 1 needed replacement wire-bond for Run 65_2. Snubber was added to input coil of J3 SQUID in Run 68.

**NEW pixels connection scheme as reported in the table**

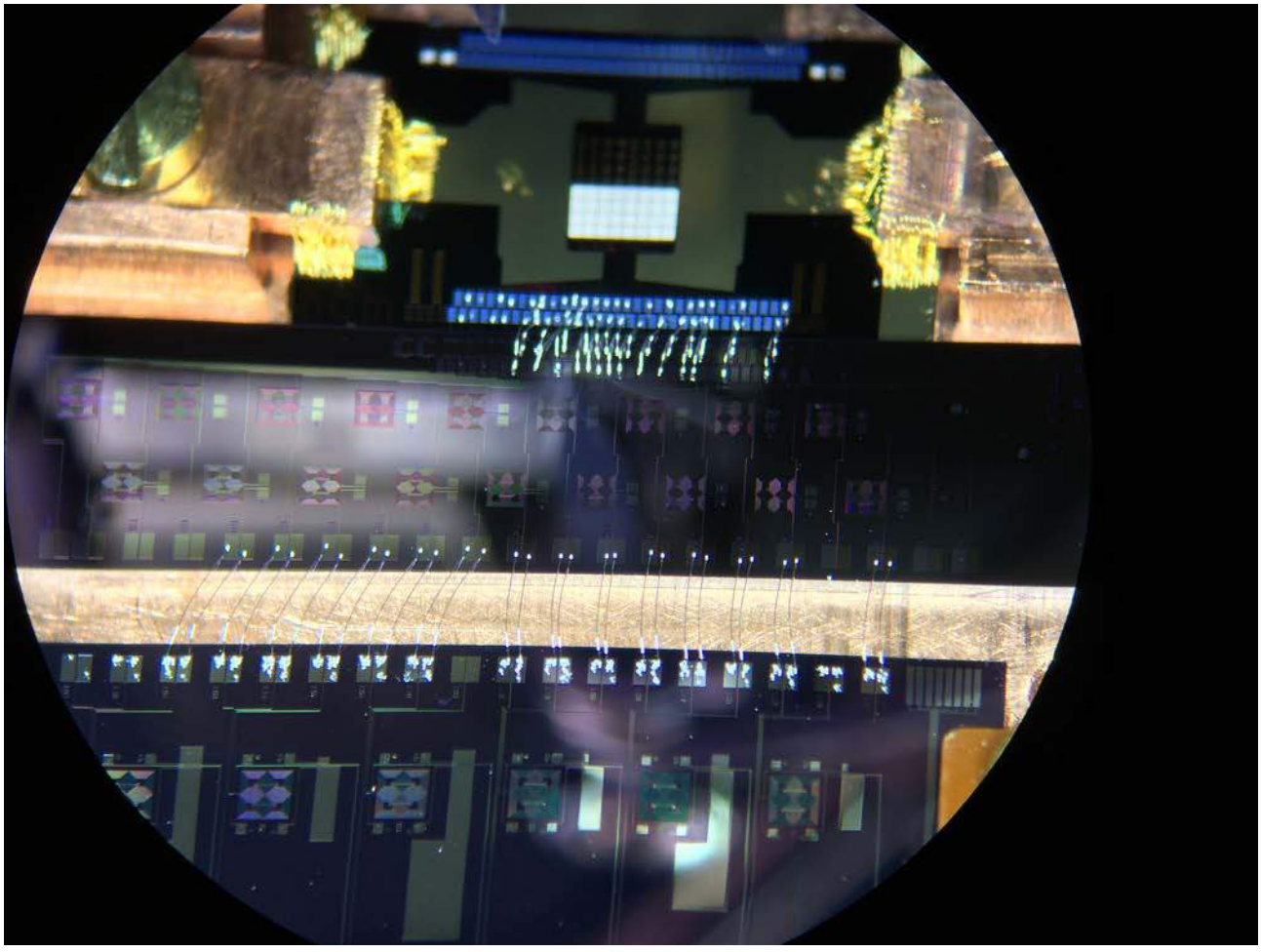


**Figure 2. New 1:2 ratio transformer chip, introduced on 10-4-2018.**

### 1.1 Overview of setup

Here an overview is given of the connected TES's and LC-resonators. The transformer chip 7b from wafer SC11-1 used is all 1:2 ratio version. Changes made this run were:

**Table 1. Wirebonding overview of TES devices (10-4-2018).**

| *LC-nr* | *Frequency (MHz)* | *Trafo nr* | *Trafo ratio* | *TES nr* | *Est. Frequency (kHz)* | *Measured Freq. (kHz)* |
|---|---|---|---|---|---|---|
| **1** | 1.1 | 4 | 2 | **8** | 1.1 | |
| **~~2~~** | ~~1.2~~ | - | 2 | | 1.2 | |
| **3** | ~~1.3~~ | - | 2 | | ~~1.3~~ | |
| **4** | 1.4 | 8 | 2 | **14** | 1.4 | |
| **5** | 1.5 | 15 | 2 | **24** | 1.5 | |
| **6** | 2 | 13 | 2 | **22** | 2 | |
| **7** | 2.7 | 7 | 2 | **13** | 2.7 | |
| **8** | 2.8 | 5 | 2 | **11** | 2.8 | |
| **9** | 2.9 | 12 | 2 | **20** | 2.9 | |
| **10** | 3 | 10 | 2 | **16** | 3 | |
| **11** | 3.1 | 18 | 2 | **31** | 3.1 | Unchanged pixel |
| **12** | 3.2 | 16 | 2 | **27** | 3.2 | |
| **13** | 4 | 11 | 2 | **18** | 4 | |
| **14** | 4.6 | 6 | 2 | **12** | 4.6 | |
| **15** | 4.7 n.c. | - | 2 | **-** | 4.7 | |
| **16** | 4.8 | 9 | 2 | **15** | 4.8 | |
| **17** | 4.9 | 14 | 2 | **23** | 4.9 | |
| **18** | 5 n.c. | - | 2 | | 5 | |

NOTE: TES,trafo and LC filters pads order from left to right on the FDMbracket is:

**TESchip : 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31**

**Trafo chip : 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20**

**LCfilter chip: 2 18 1 8 14 7 4 16 3 10 13 9 6 17 5 12 15 11**

### 1.2 Trafo chip SC11-1 7b (1:2 48nH)

In run 71 a new transformer chip was introduced on the Probe, with a yield of 18/18 expected from room temperature measurements. To minimize the stray inductance effect, the transformer chip was placed as close as possible to the TES array. This resulted in a bigger gap between the LC-filter chip and Trafo chip, but longer bond wires here should have a negligible stray inductance effect as the secondary coil and LC-filter inductance are above 2uH while the primary trafo coil is 48nH.

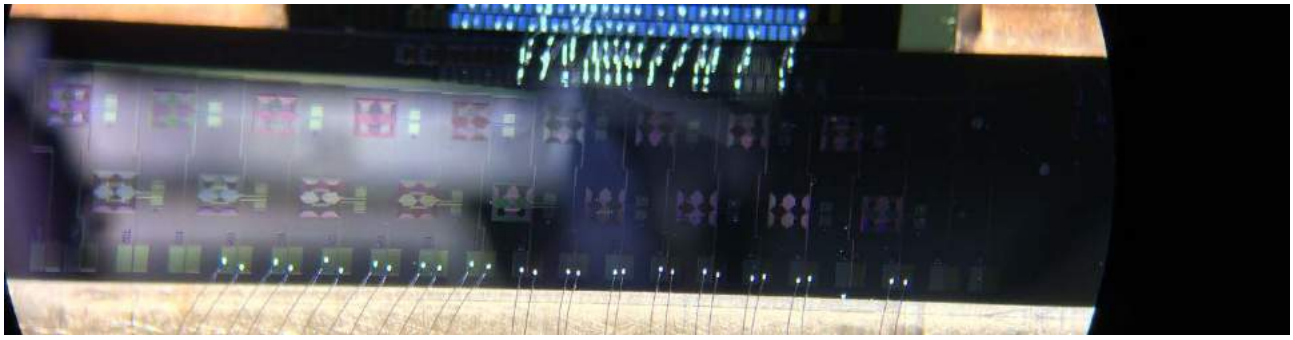


**Figure 3. Trafo chip, with 1:2 ratio transformers, as introduced in Run 71, 10-4-2018.**

### 1.1 Wafer LC17-6 Chip 2 (18-pixel; 2 µH)

| | # OK | Remarks |
|---|---|---|
| TES input strip-line | 18 | O.L. (> 40 MΩ) |
| Bias summing point | | 15 MΩ |
| Squid summing point | | O.L. |
| Capacitors | 17 | C03 = 3.5 kΩ |
| Bias capacitors | 18 | |
| Coils | 18 | From optical inspection. Value around 140 kΩ |

Chip can be used for 17 pixels

An extra dicing step was necessary to make the chip fit on the Cu-bracket, this was done with great help from Kenichiro Nagayoshi.

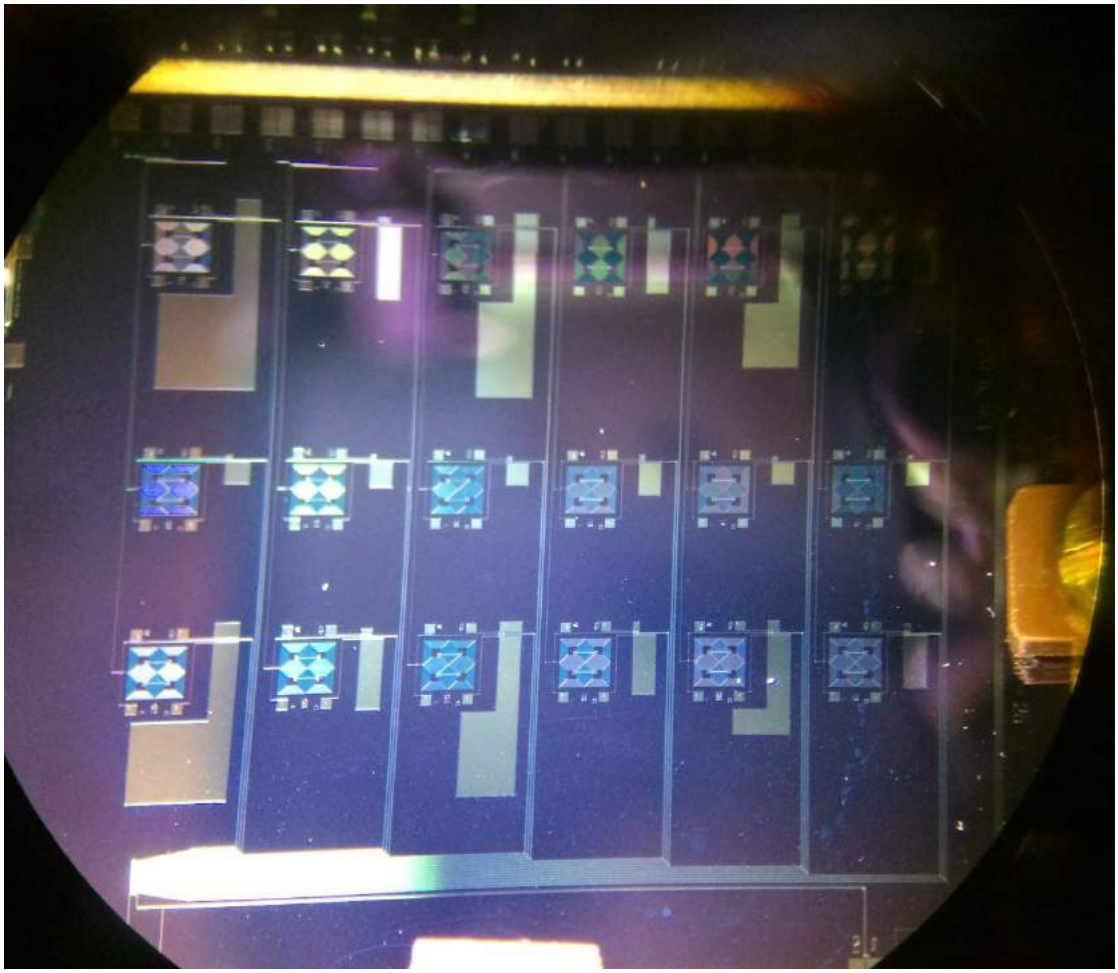


**Figure 4. LC filter after mounting on the copper bracket.**

### 1.2 Goddard A5 mixed TES array

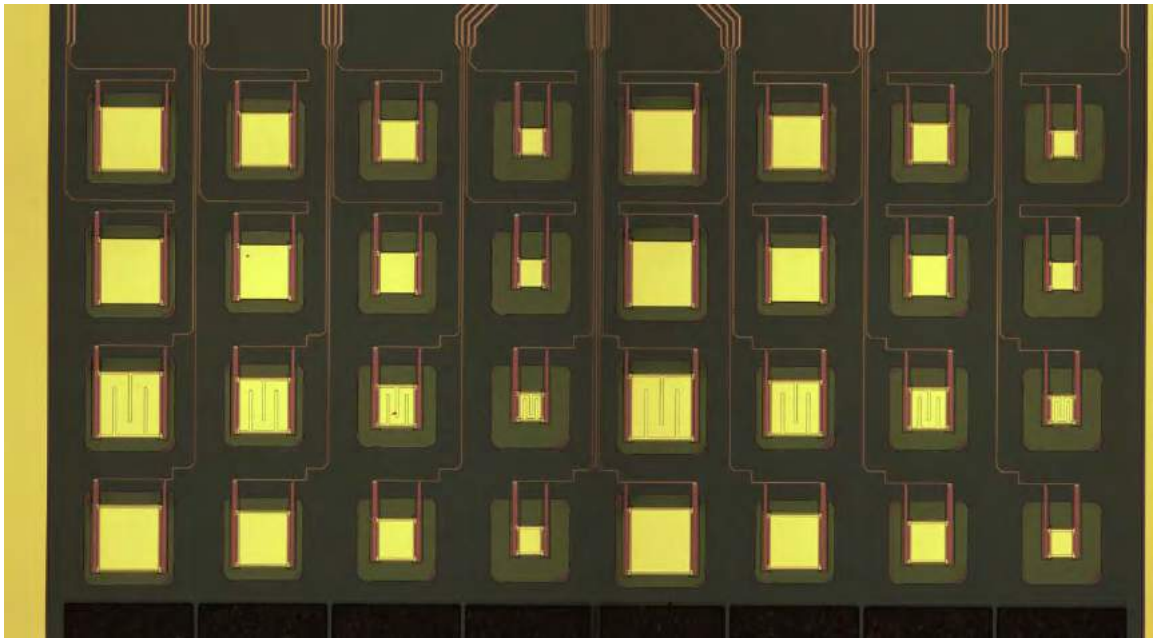


**Figure 5. GSFC A5 array, zoom of TES structures.**

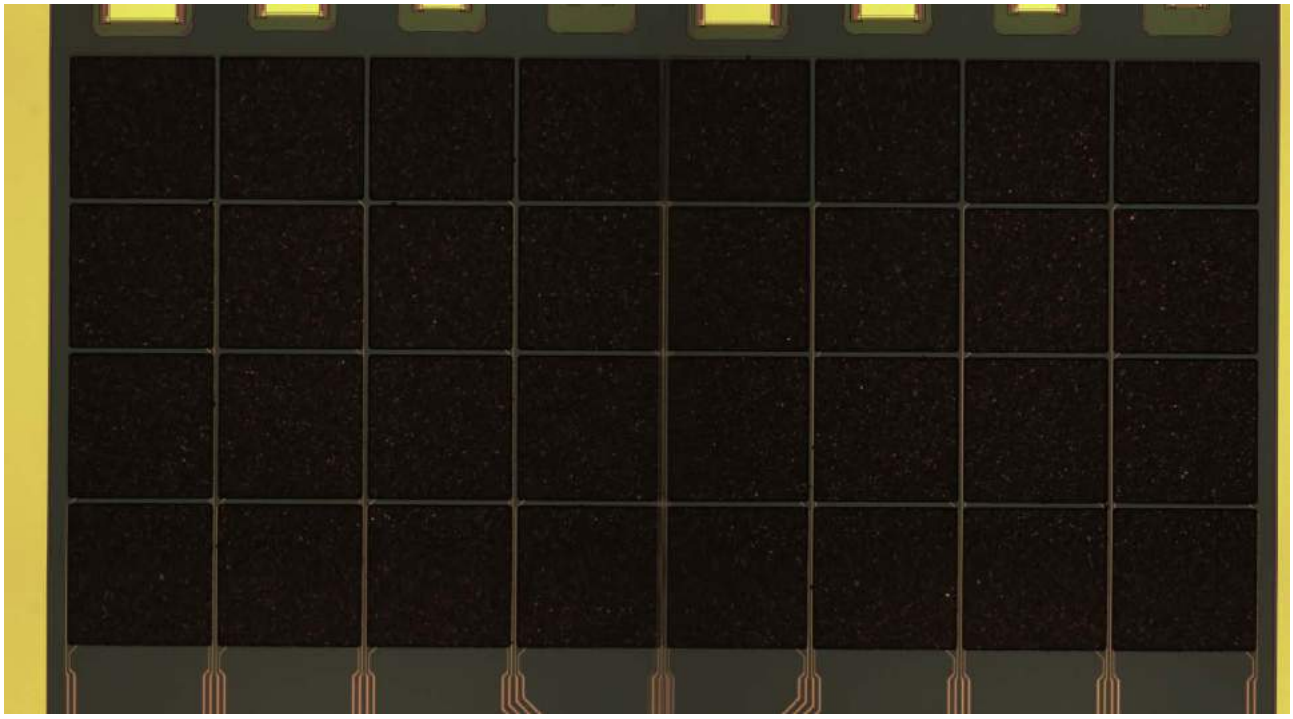
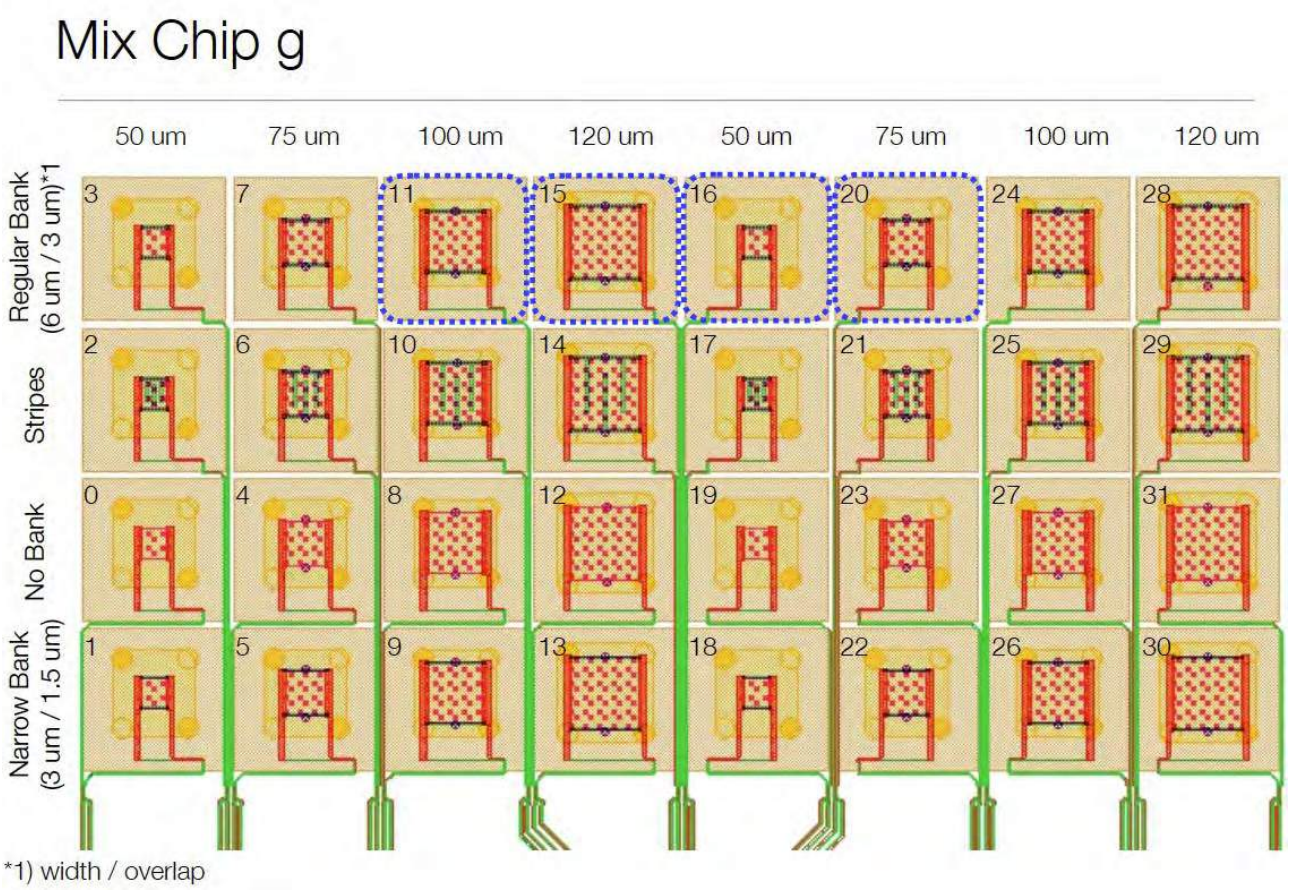


**Figure 6. GSFC A5 array, zoom of absorbers.**

# Wafer 17.6

- Athena-1 G
- PVD
- 0.5 um membrane
- Au 2.30 um (50% more than nominal) / Bi 3.39 um

| TES Ch | TES Size (um) | Stripes | Tc (mK) | Rn (mOhm) | G@Tc (pW/K) | C@Tc (pJ/K) |
|---|---|---|---|---|---|---|
| 15 | 120 | 0 | 84.6 | 32.7 | 125 | 0.95 |
| 11 | 100 | 0 | 84.4 | 30.4 | 104 | 0.91 |
| 20 | 75 | 0 | 84.9 | 25.8 | 77 | 0.84 |
| 16 | 50 | 0 | 86.6 | 22.4 | 59 | 0.86 |




TES 0 & TES 19 should not be connected.

### 1.3 Snubber - or lowpass RC-filter at Input SQUID

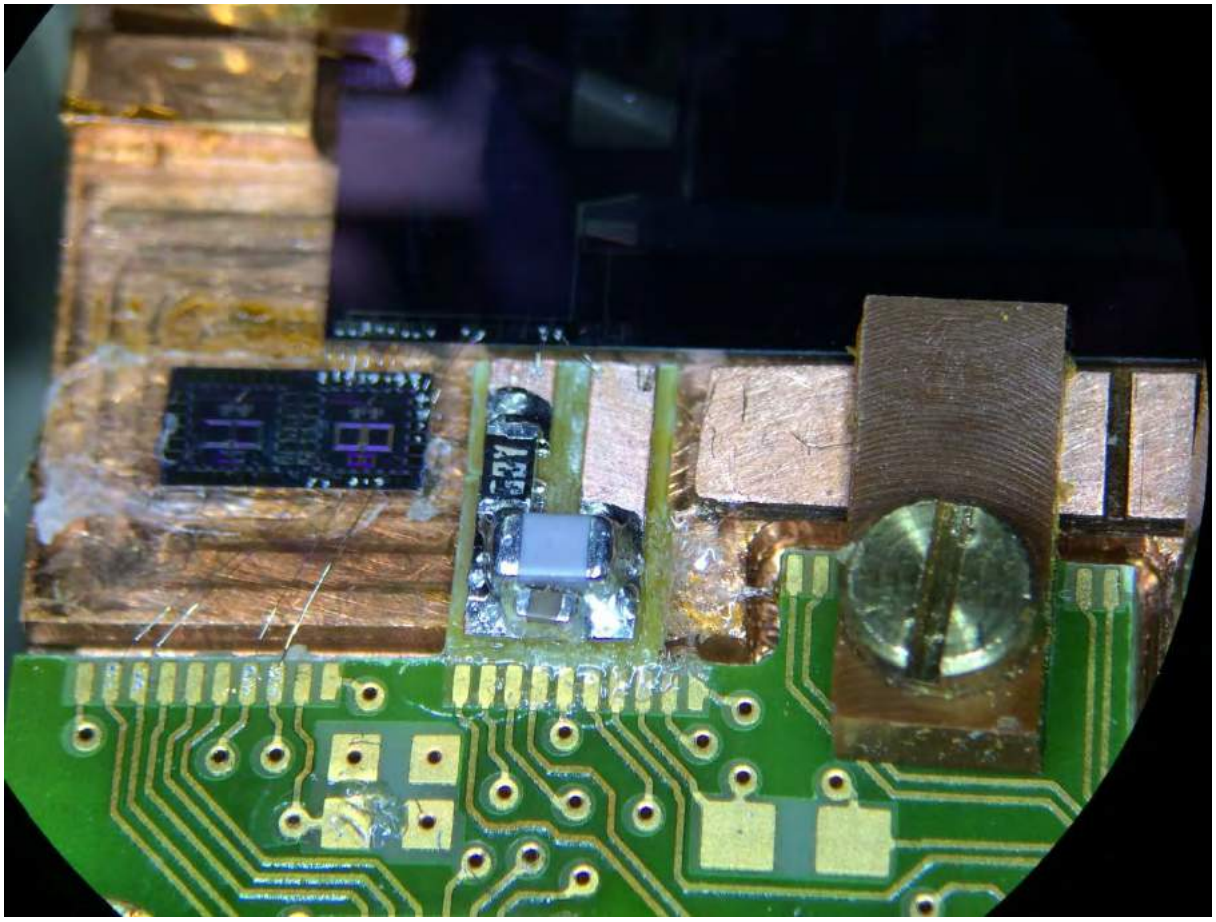
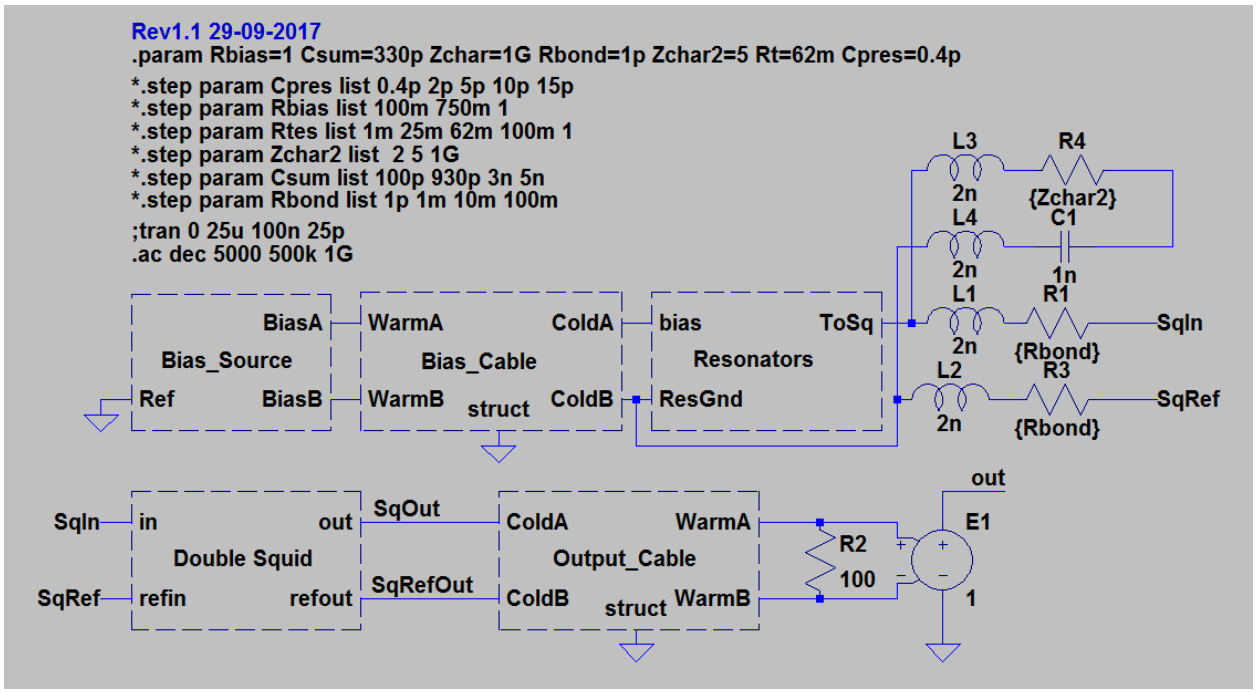


**Figure 7. Snubber / lowpass RC-filter circuit in parallel with Input SQUID.**

The snubber consists of a 5Ohm (see Zchar2) resistor and 1nF (see C1) with a 1pF (not needed in model, see figure above). Introduced in Run 68, connected to the summing point of the LC-filter chip.



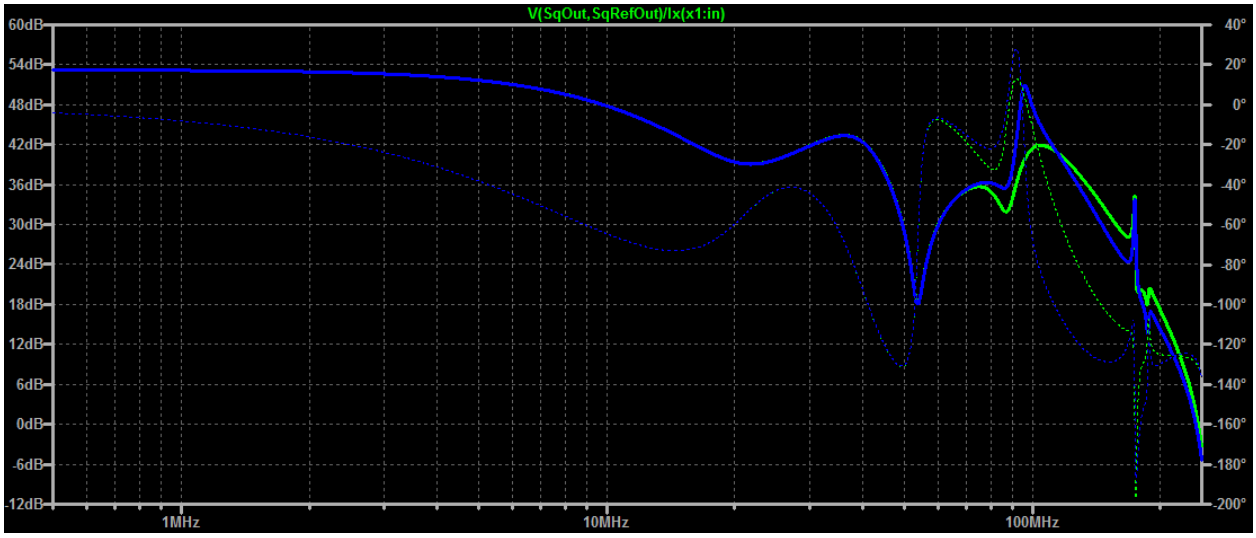




**Figure 8. Two SQUID transfer, between I_SqIn and V_SqOut, with snubber on input SQUID (Green). Without snubber (blue) shows a strong 100MHz oscillation.**

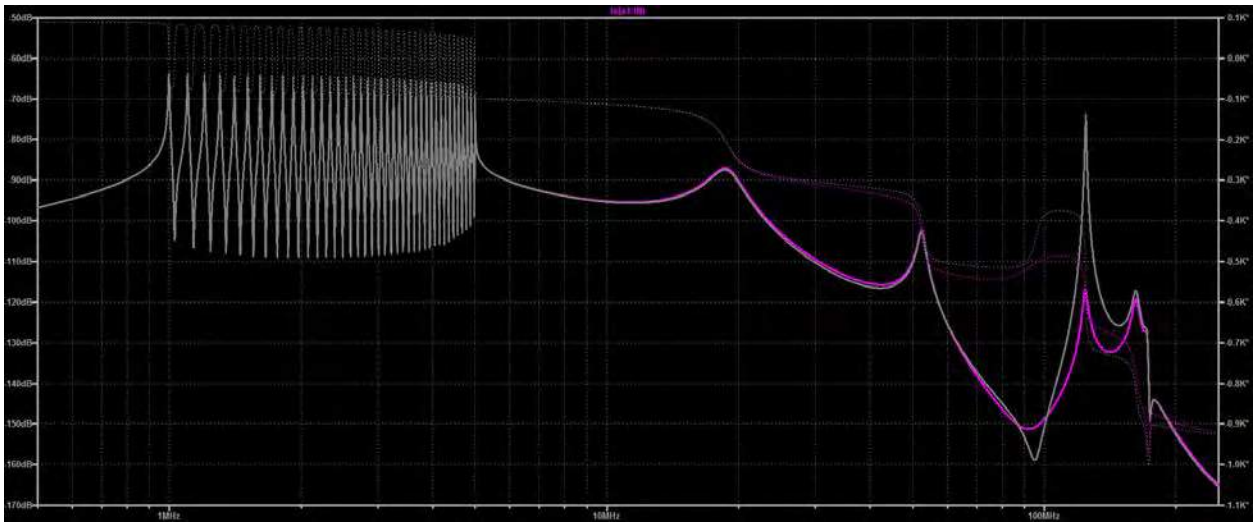


**Figure 9. Current probed at Input SQUID (input coil), without snubber (grey line) with snubber (magenta line).**

### 1.4 Pictures

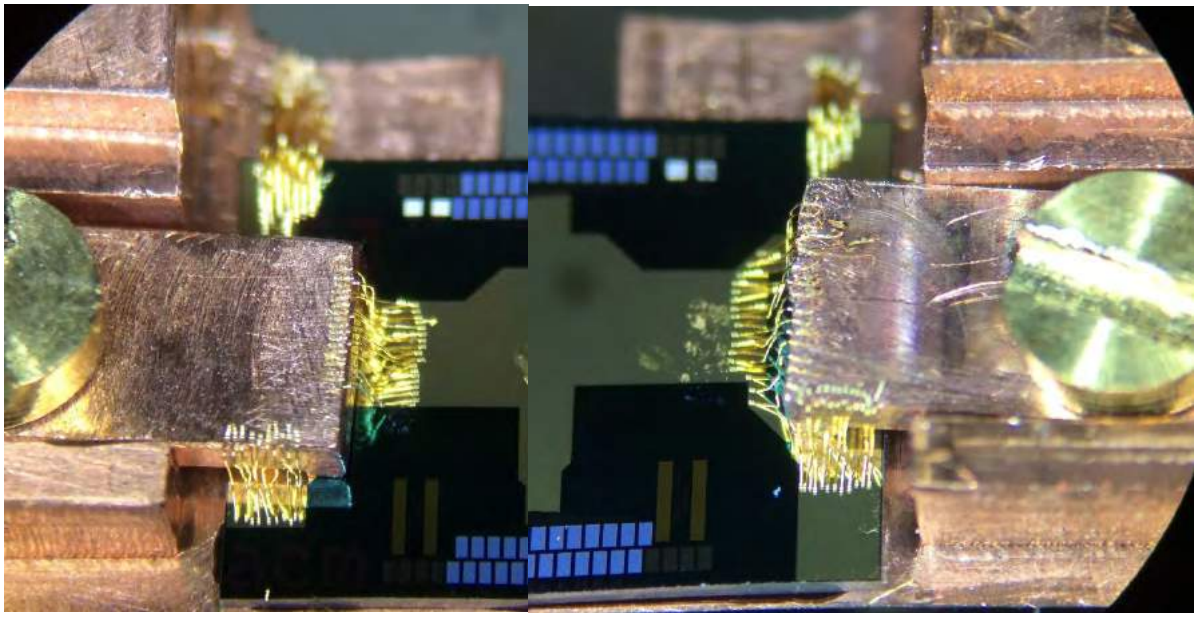


**Figure 10. Au-thermalization wire-bonds.**

## Appendix 3
## FDM_large setup overview

**Wirebonding Report: (X)FDM_Large setup Run Groningen 12 – Cooldown94**
**Prepared by: Kevin Ravensberg, Pourya Khosropanah, Kenichiro Nagayoshi, Emanuele Taralli**

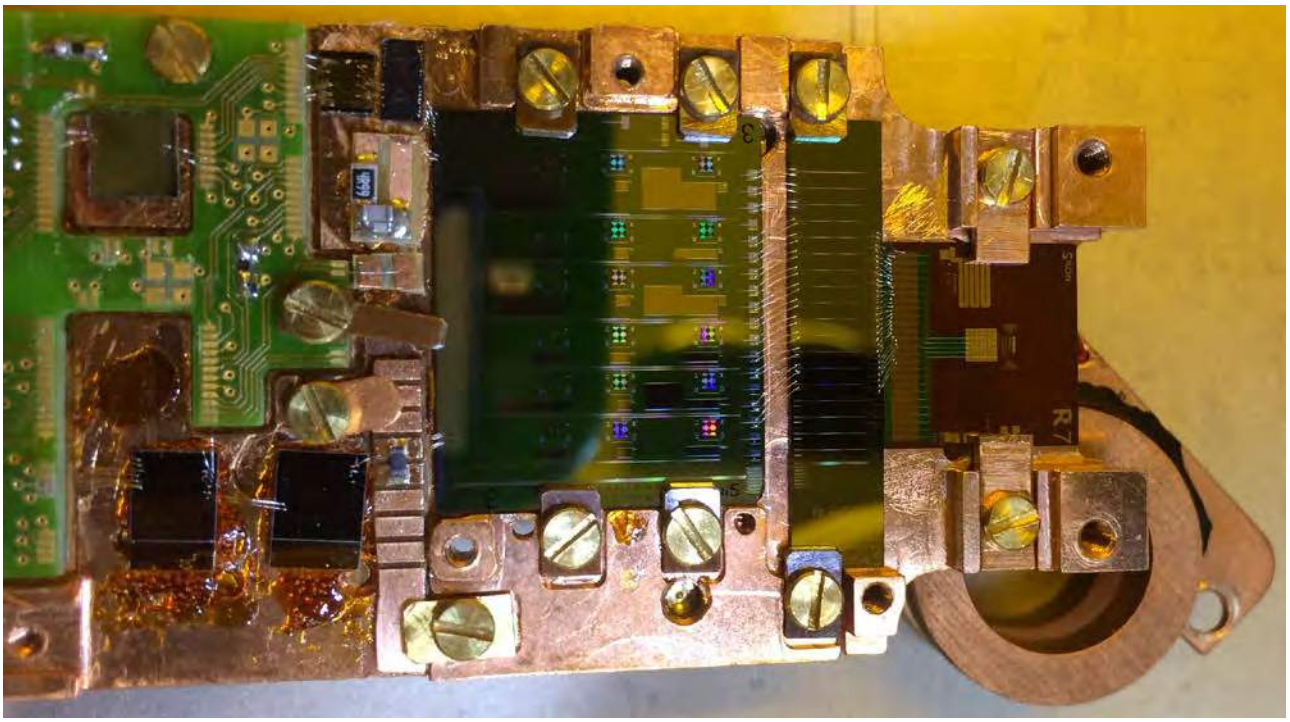


**Figure 1. New SRON TES calorimeter array R7 installed for run G12.**

***Table of contents:***

## 1 Modification overview:

In run G12 a new SRON TES array is introduced, with 120um 100um and 80um sized devices.
We introduced LC-filter 17-12 chip 3, dc-interconnect SC07-2 Chip 4a to have enough channels for all available TES devices and minimize read-out problems with a Snubber at the Input SQUID input-coil.
The J3 input SQUID is new and F5 output SQUID on the cold-finger is as before, the TES array has been left untouched and **Fe55** X-ray **source #1** is installed on the Al-shield of this setup since February 2017 (Willem-Jan Vreeling can be contacted for info on this source).

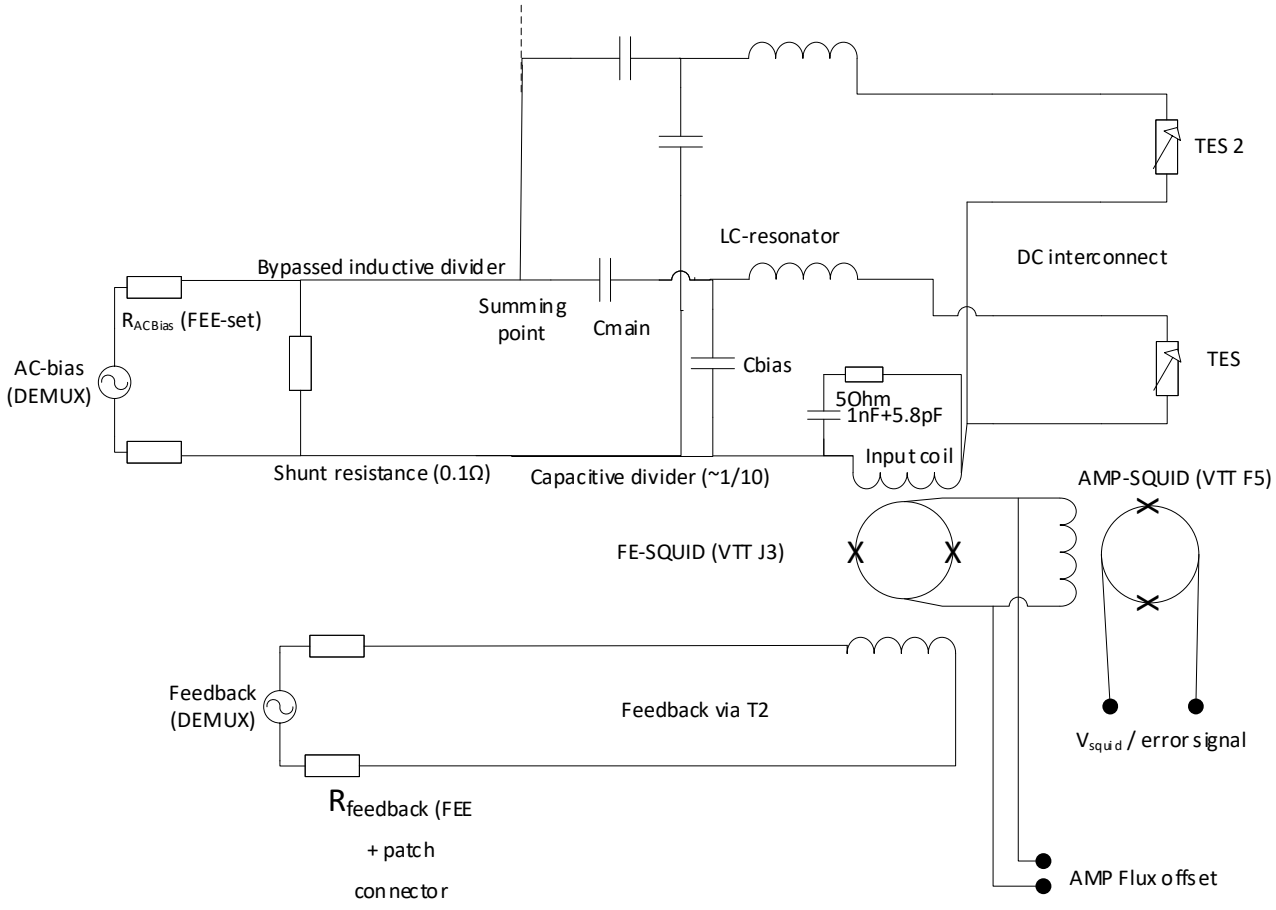



**Figure 2. Circuit diagram of LC resonators / TES between AC-bias and input SQUID.**

The routing of the AC-bias and Feedback lines are still changed in the looms of the LC-cooler, by a patch in the Cryo-patch PCB mounted next to the setup.

### 1.1 SRON TES array

SRON TES array R7, 120um 100um and 80um devices are connected.

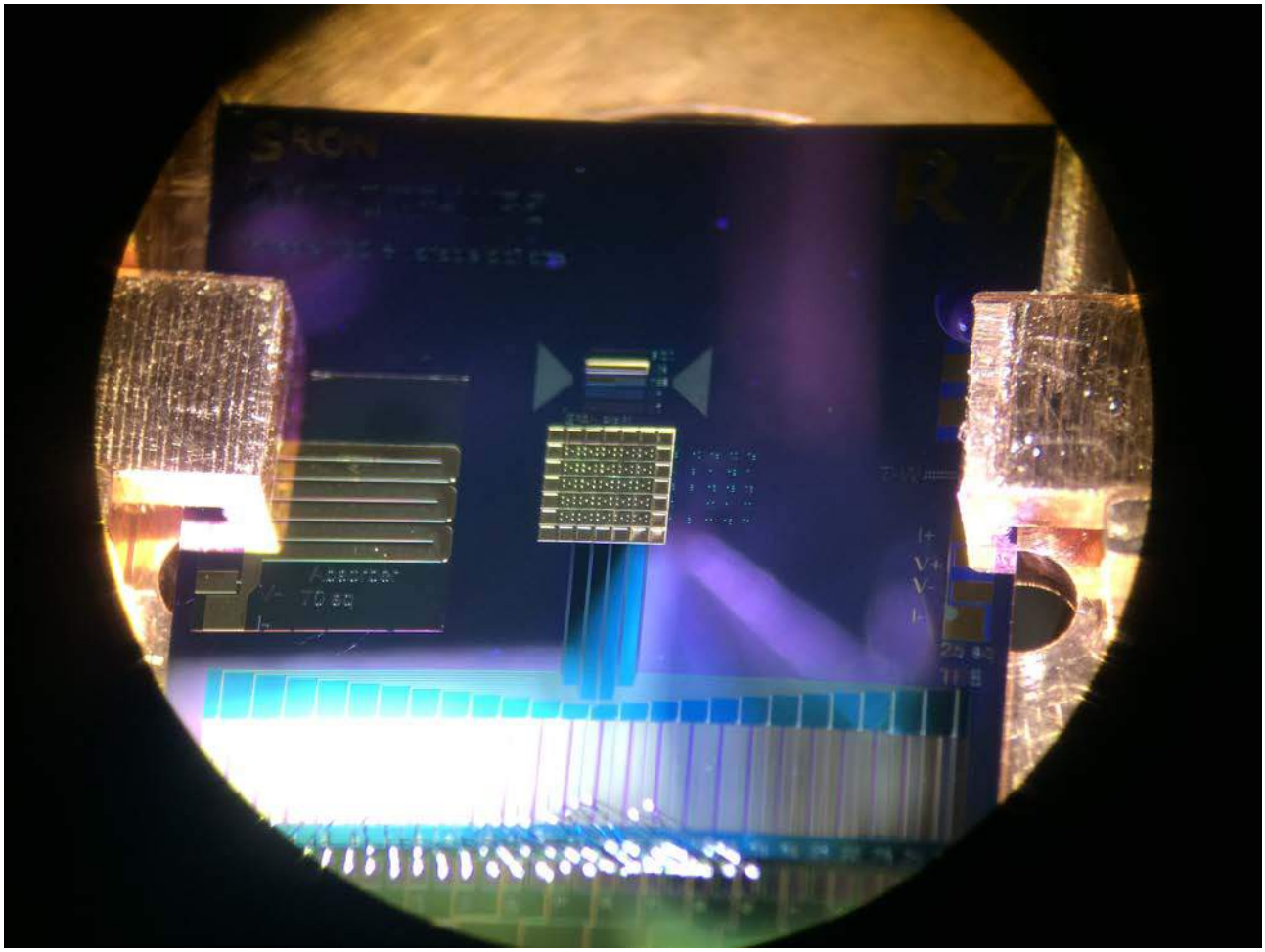



**Figure 3. SRON TES array R7 (wafer ?), with full Au-absorbers in center 5x5**

TES devices 14, 16~25 are not usable on this array and should not be connected!

### 1.2 Thermalisation wirebonds

No Au-wire bonds have been placed on this array, as this array has a copper thermalisation layer on the back of the chip already and no bondable gold surface on the top.

### 1.3 J3 SQUID placed

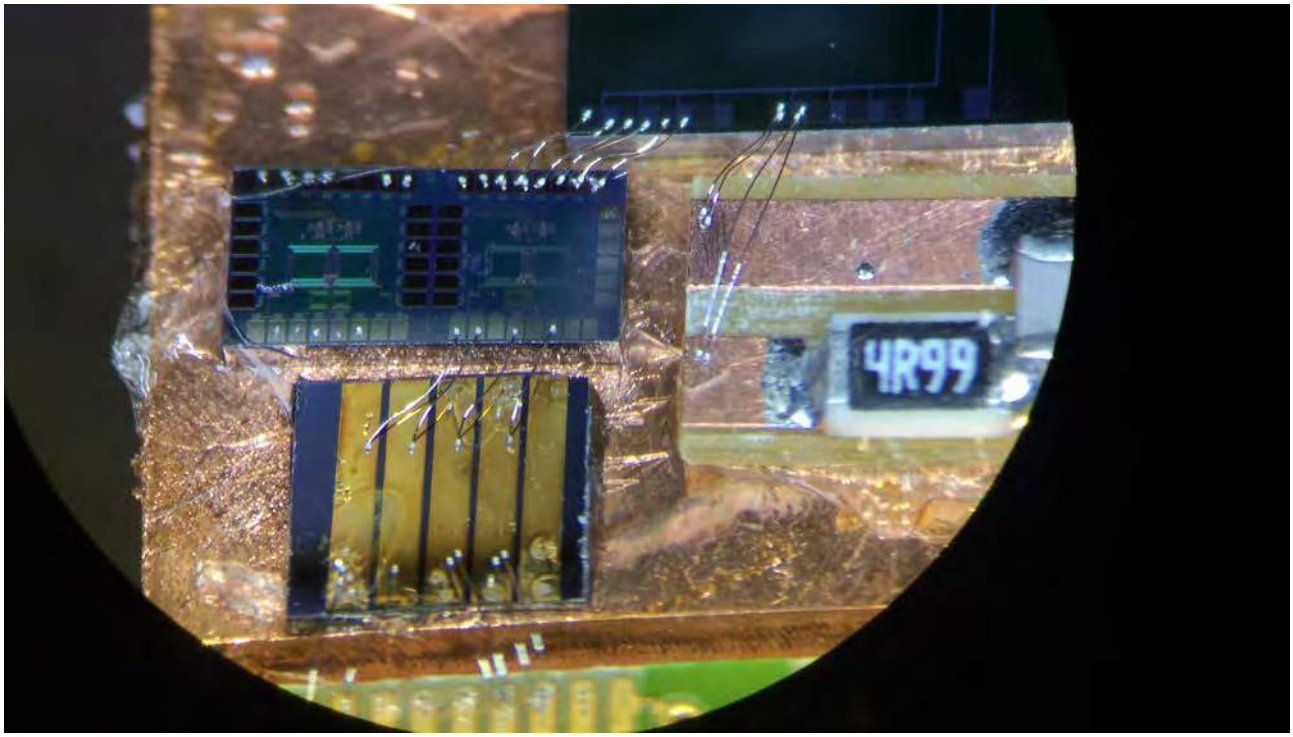



**Figure 4. J3 input SQUID ret R, as of 26-4-2018.**

This SQUID has worked in the previous runs, left as it was for Run G6. In Run G12 the connection to the summing point on the LC-chip was redone, as the LC-chip was replaced for a newer version with summing point on chip.

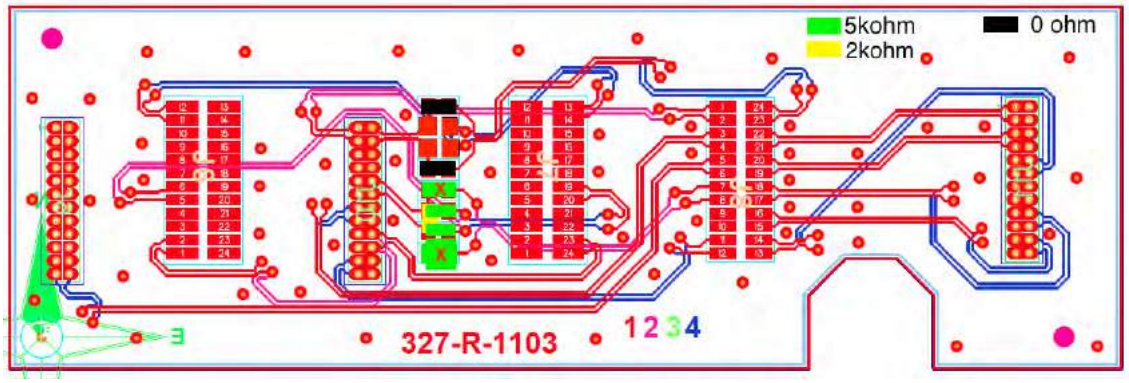



**Figure 5. New FEE-patchboard layout, required to apply feedback via Loom 1 (wire 3-4).**

### 1.4 AMP-SQUID cold finger (no changes for Run 58 or Groningen 1, Groningen 2)

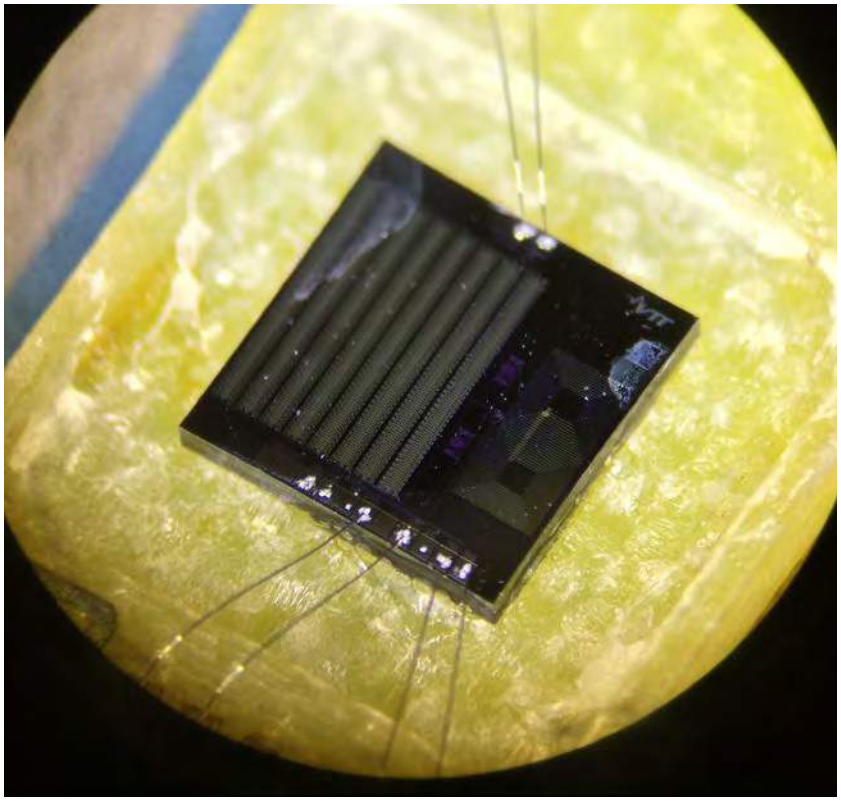



**Figure 6. AMP SQUID (VTT F5 - IGG#3) on cold finger PCB.**


**Figure 7. Cold finger PCB overview.**

The 10-pin loom connector was connected with nr 1 indicating triangle at the middle of the cylinder circle.

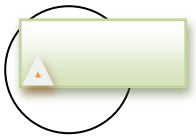


**Figure 8. Connector position on cold finger, triangle indicates loom nr 1.**

**Table 1. Ohm-out of resistances at 300K / room temperature.**

| Cold Finger signal | loom (10-pin) | R (kOhm) | J8 cryopatch-board |
|---|---|---|---|
| AMP SQUID V+- | **2 3** | 3.510 | 8 9 |
| AMP Fx_1 +- | **10 1** | 28.910 | 1 10 |
| FE SQUID bias | **5 4** | 0.051 | 6 7 |
| AMP input coil | **(4pins male)** | 96.800 | *to bracket* |

## 2 Wirebonding overview

No change to the LC-filter (1000nH coils) has been made for Run G6, faulty/broken LC's are # 8.
No transformer chip is needed for the TES's and LC filter combination. DC-interconnect chip SC07-2 chip 4a was introduced in run G12, together with LC17-12 chip 3 (18nm a-Si Phillips). No defects were found on the interconnect chip, but LC08 has a missing top wire section between summing point and LC-resonator and should not be used.

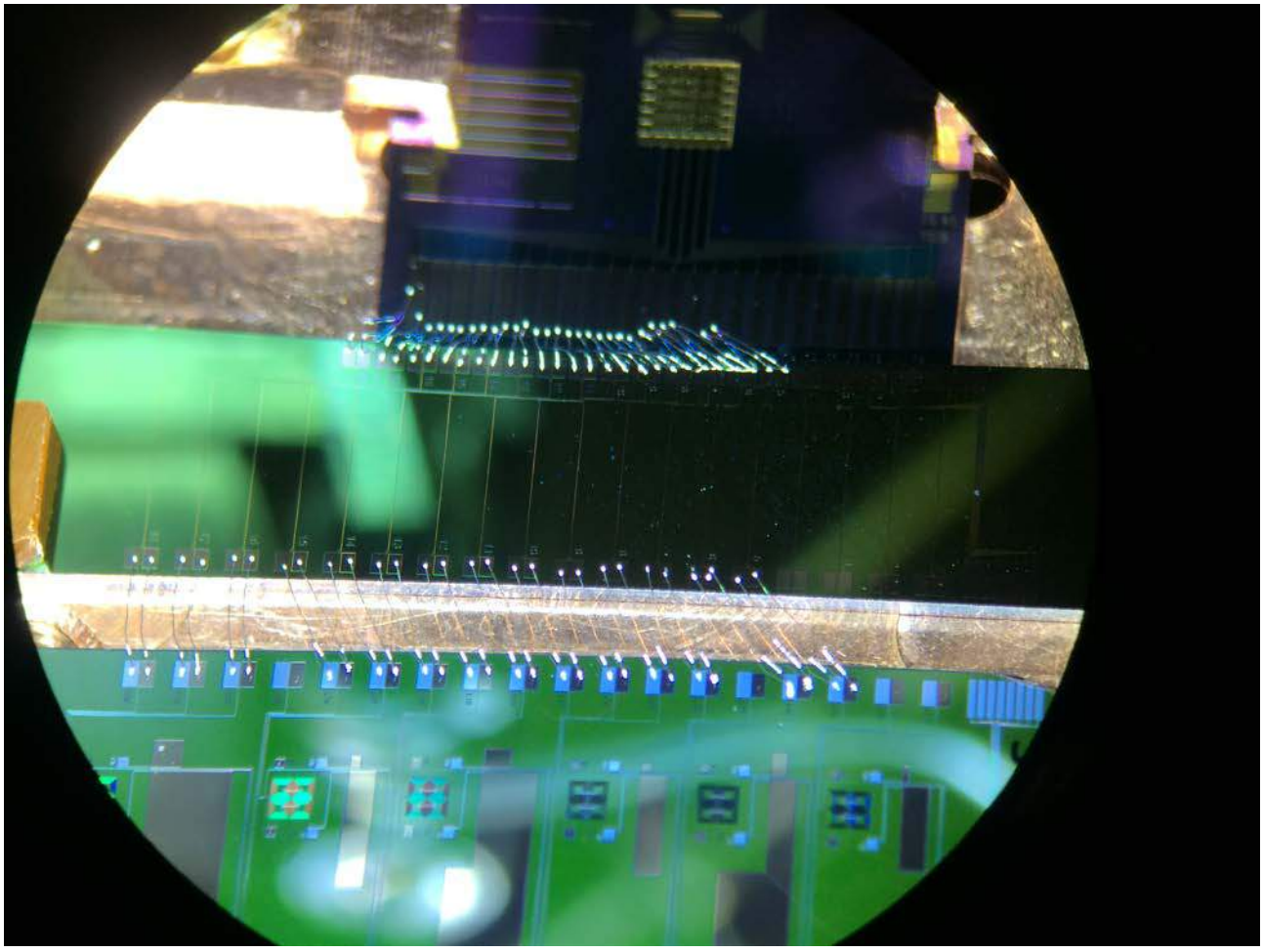


**Figure 9. Al-wire bond connections between LC-filters, DC-interconnect and TES array, 26-4-2018.**

### 2.1 Overview of setup

New frequency distribution, real frequencies will be ~100kHz lower than designed frequency.

**Table 2. Wirebonding overview of TES devices, 26-04-2018.**

| *LC-nr* | *Design Frequency (kHz)* | *Stripline nr* | *TES nr* | *Expected Frequency (kHz)* |
|---|---|---|---|---|
| 1 | 1100 | 16 | **3** | 1000 |
| 2 | 1200 | 18 | **1** | 1100 |
| 3 | 1300 | 11 | **8** | 1200 |
| 4 | 1400 | 13 | **6** | 1300 |
| 5 | 1500 | 6 | **13** | 1400 |
| 6 | 2000 | 7 | **12** | 1900 |
| 7 | 2700 | 14 | **5** | 2600 |
| 8 | 2800 | - | | |
| 9 | 2900 | 8 | **11** | 2800 |
| 10 | 3000 | 10 | **9** | 2900 |
| 11 | 3100 | - | | 3000 |
| 12 | 3200 | 5 | **15** | 3100 |
| 13 | 4000 | 9 | **10** | 3900 |
| 14 | 4600 | 15 | **4** | 4500 |
| 15 | 4700 | - | | |
| 16 | 4800 | 12 | **7** | 4700 |
| 17 | 4900 | - | | |
| 18 | 5000 | 17 | **2** | 4900 |

## 3 Cu-collimator plate

A new collimator plate was made and is used in run Groningen 2 (cooldown 81). The aperture in this plate was filled to match the exact location of the detector array on chip. With the R7 array this collimator chip still should work, but it exposes a larger area of substrate around the array to X-rays.

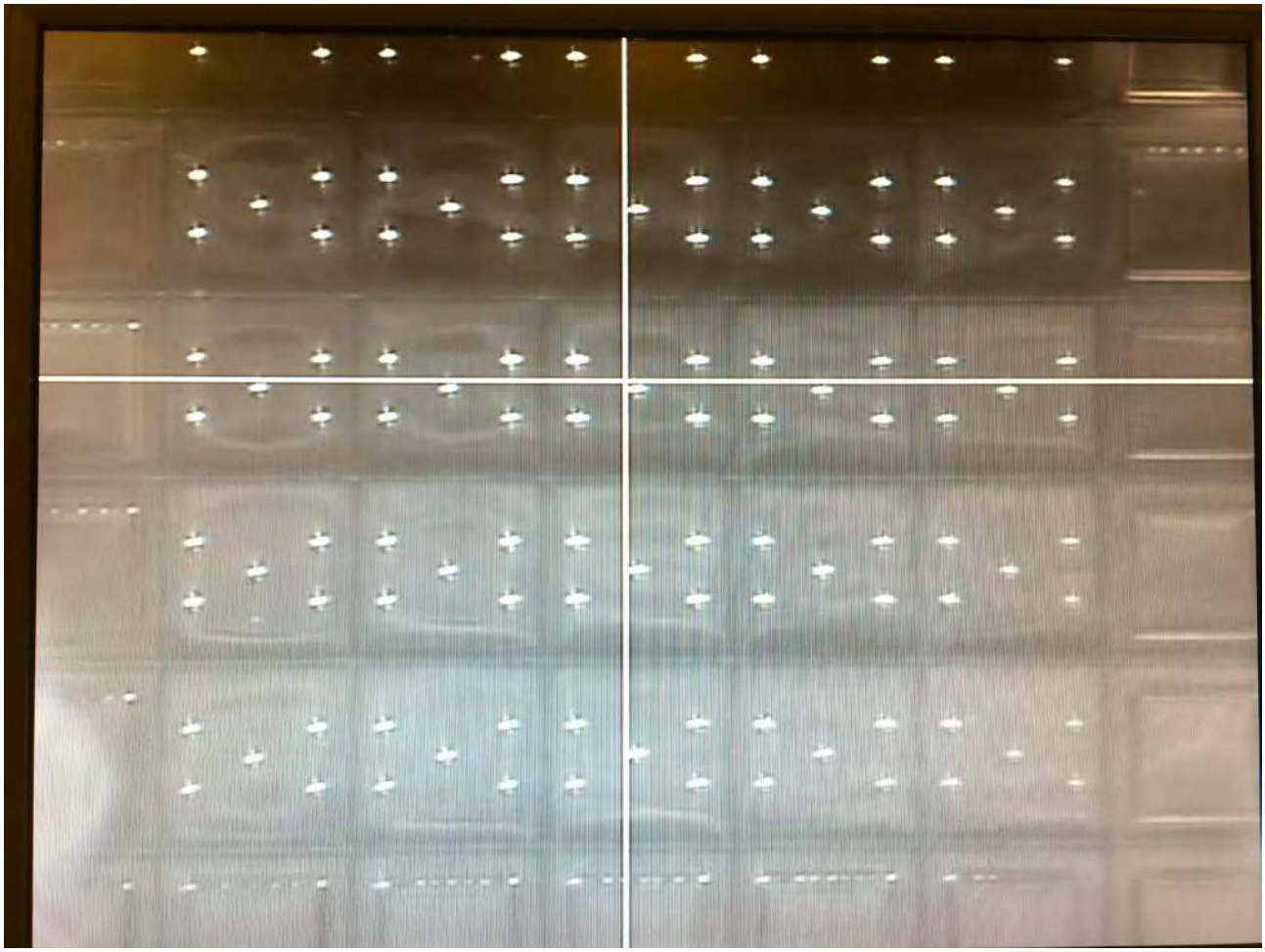


**Figure 10. TES array viewed through collimator plate from camera top-view.**

## 4 Snubber

A RC-lowpass filter has been introduced at the input coil of J3/Input SQUID, also known as a snubber. The chip has a 5 Ohm resistance in series with a 1nF // 5.8pF capacitance and should filter strongly for frequencies above 10MHz between the LC-filter and SQUID.

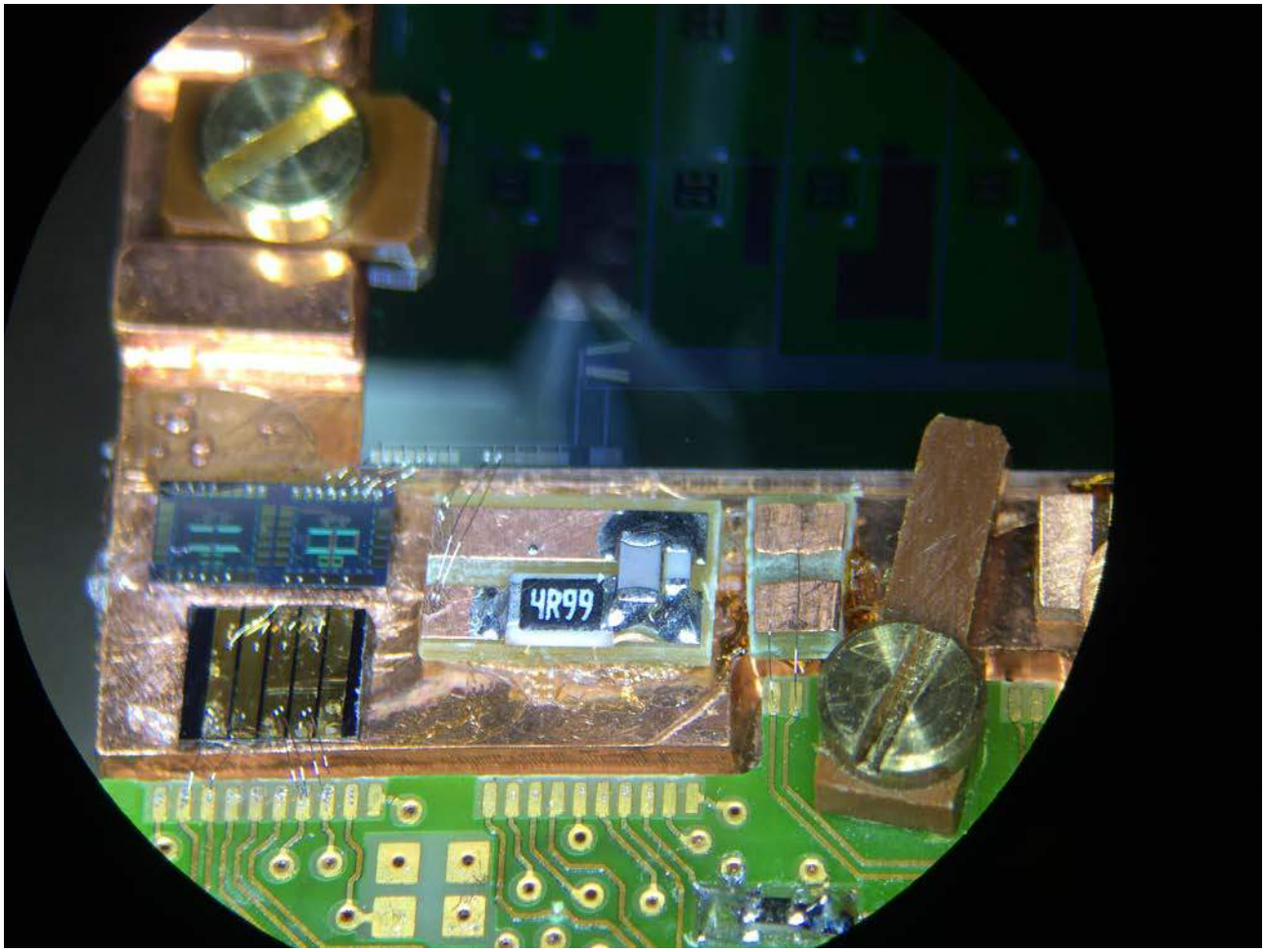



**Figure 11. Snubber chip introduced in run G12, 26-4-2018.**

## Appendix 4
## 40-pixel-A setup overview

| SRON / IFU | REPORT | **Doc. no.** : SRON-XIFU-RP-2017-023<br>**Inst. no.** :<br>**Issue** : 1.01<br>**Date** : 23 February 2018<br>**Cat** :<br>**Page** : 1 of 23 |
|---|---|---|

**Title : 40 Pixel FDM wire-bonding report**


**Prepared by** : Kevin Ravensberg **Date** : 13-4-2018

**Checked by** : **Date** :

**PA agreed by** : **Date** :

**Authorised by** : **Date** :


**Distribution**

Hiroki Akamatsu
Luciano Gottardi
Jan van der Kuur
Ruud Hoogeveen
Rob Wolfs
Dennis van Loon
Marcel van Litsenburg
Johannes Dercksen

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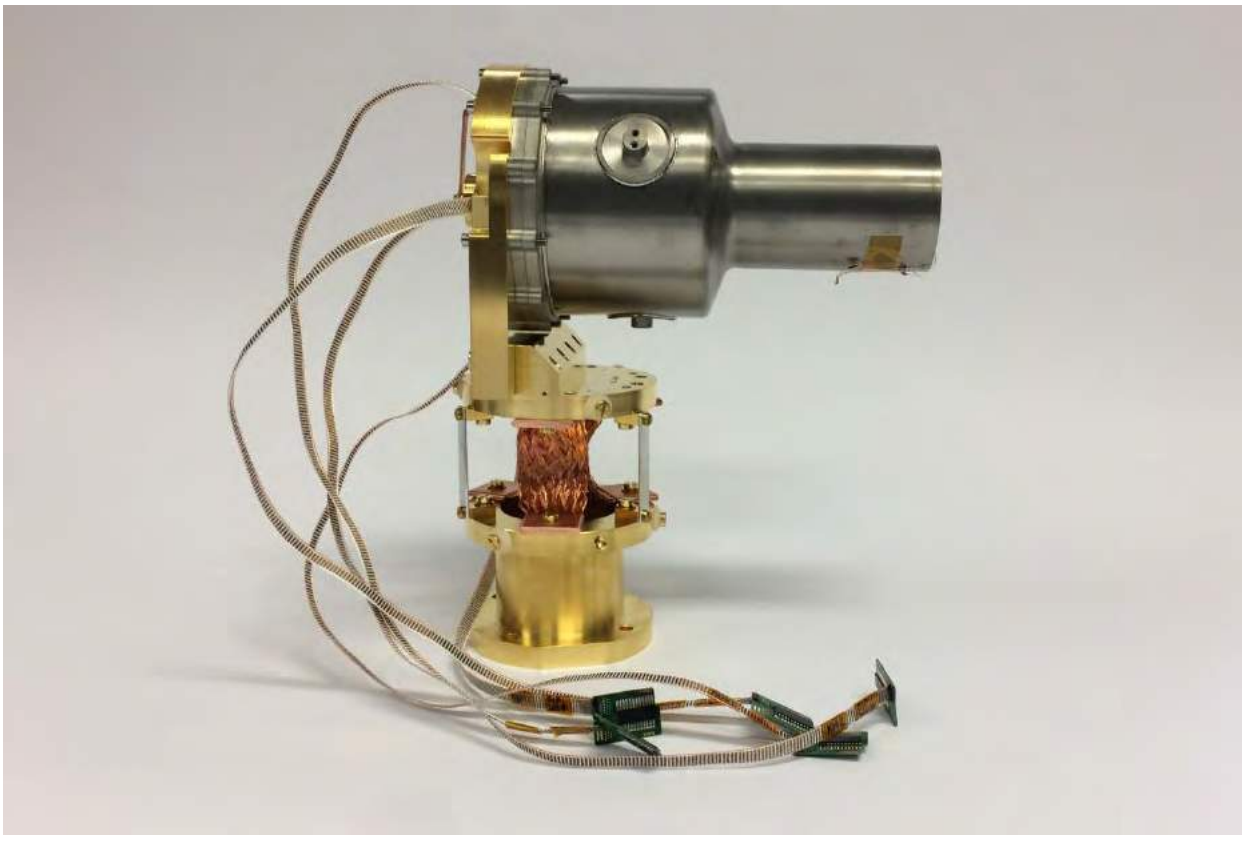


## Abbreviations and acronyms

| Item | Meaning |
|---|---|
| FDM | Frequency Domain Multiplexing |
| GSFC | NASA Goddard Space Flight Center |
| SQUiD | Superconducting Quantum Interferrence Device |

## Reference Documents

| [RD#] | Doc. Reference | Issue | Title |
|---|---|---|---|
| [RD1] | SRON-XIFU-RP-2016-003 | 1.0 | **Measurement report LC 17-1** |
| [RD2] | SRON-XIFU-RP-2016-005 | 1.0 | **Measurement report Trafo chip SC10-3** |
| [RD3] | | | |
| [RD4] | | | |
| [RD5] | | | |
| [RD6] | | | |

## 1 Introduction

In this document the status of all connected devices for each 40px experiment run/cooldown will be documented, a new version will be made for every run and stored in the respective folder on: https://owncloud.sron.nl/owncloud/index.php/s/YVW5erIjbQHgHtP

## 2 Wire-bond overview

This is an overview of the connected SQUID's, LC-filters and TES devices for the ninth cool down of the **40 pixel FDM - A** experiment. Previously the LC-filters have been connected to the input SQUID and the ACbias shunt resistance had been increased from **0.27** to **1.0** Ohm, to prevent unmanageable Q-factors (we damp the intrinsic Q-factor that reached > 100 000). 31/36 available LC-filters have been connected to TES's, see the table below for a detailed overview. Due to an issue with the SQUIDs in the setup, we re-did the wire bonding of the Input SQUID in Run 64. This did not solve the issue so in Run 65 we re-did the Output SQUID wire bonding too. Here we discovered that one of the Au-wires to the Output SQUID input coil was only loosely laying on the Cu bond-pad on the PCB, not properly connected anymore as was the case in Run 62. In Run 67 one of the LC-channels (LC05 with trafo #20 and TES#30) has been removed, it showed strange behaviour at 50mK (no response to small excitation currents). Kevlar suspension has been added in Run 67.

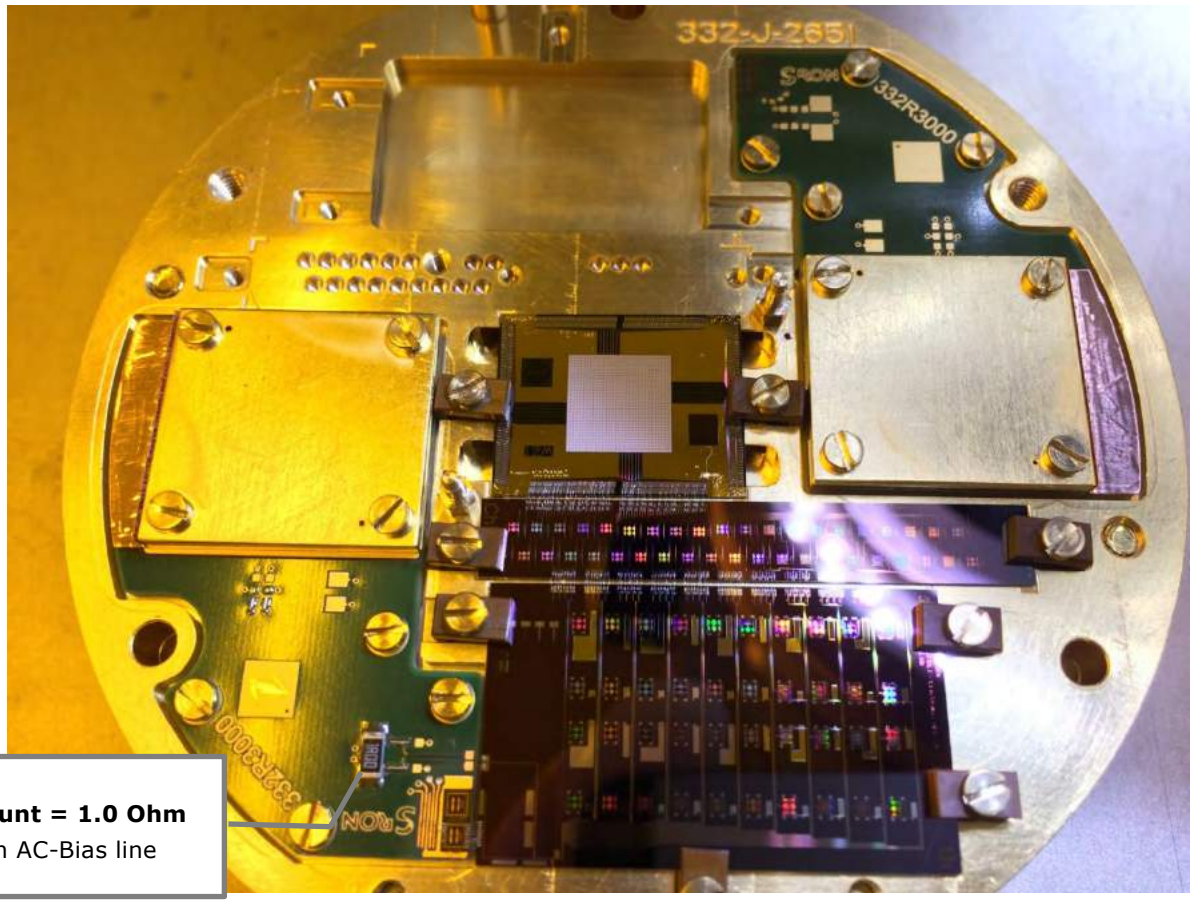



**Figure 1. Overview picture of the 50mK bracket of 40 Pixel FDM - A for Cooldown 5, LC Run63.**

| LC filter # | Trafo # | TES # | Design frequency (MHz) | Frequency measured (kHz) | Q-factor fitted | comments |
|---|---|---|---|---|---|---|
| **1** | 4 | **6** | 1.1 | 1066.726 | 8293.98 | |
| **2** | 2 | **2** | 1.2 | 1167.505 | 8895.21 | |
| **3** | 12 | **17** | 1.3 | 1261.223 | 9913.15 | |
| **4** | 10 | **15** | 1.4 | 1359.482 | 9847.77 | |
| **5** | 20 n.c. | **30 n.c.** | 1.5 | 1454.768 | 11140.68 | Removed in Run 67 |
| **6** | 18 | **28** | 1.6 | 1553.113 | 11266.75 | Changed in Run 71 |
| **7** | 28 | **43** | 1.7 | 1649.043 | 11311.80 | |
| **8** | 26 | **40** | 1.8 | 1747.959 | 12736.83 | |
| **9** | 36 n.c. | | 1.9 | 1844.399 | 13619.81 | Possibly connect 56 |
| **10** | 34 | **53** | 2 | 1944.873 | 14289.61 | |
| **11** | 8 | **11** | 2.1 | 2037.962 | 13898.44 | |
| **12** | 6 | **8** | 2.2 | 2136.707 | 13717.85 | |
| **13** | 16 | **24** | 2.3 | 2232.059 | 16501.39 | |
| **14** | 14 | **21** | 2.4 | 2328.009 | 15792.68 | |
| **15** | 24 | **37** | 2.5 | 2421.977 | 15967.29 | |
| **16** | 22 | **34** | 2.6 | 2524.459 | 18570.99 | |
| **17** | 32 | **49** | 2.7 | 2621.812 | 19069.16 | |
| **18** | 30 | **47** | 2.8 | 2722.982 | 20586.39 | |
| **19** | 40 n.c. | | 2.9 | 2816.389 | 18235.51 | Possibly connect 63 |
| **20** | 38 n.c. | | 3 | 2921.631 | 18690.02 | Possibly connect 59 |
| **21 (coil)** | 29 n.c. | | 3.1 | ? | ? | Not connected (open at trafo side) |
| **22** | 31 n.c. | | 3.2 | ? | ? | Missing? Check! |
| **23** | 37 n.c. | | 3.3 | 3210.415 | 21599.60 | Possibly connect 57 |
| **24** | 39 n.c. | | 3.4 | 3306.711 | 22561.51 | Possibly connect 60 |
| **25** | 21 | **33** | 3.5 | 3398.992 | 22288.09 | |
| **26** | 23 | **36** | 3.6 | 3494.01 | 21982.83 | |
| **27** | 13 | **19** | 3.7 | 3593.995 | 23642.05 | |
| **28** | 15 | **23** | 3.8 | 3693.249 | 22878.23 | |
| **29** | 5 | **7** | 3.9 | 3790.974 | 25278.17 | |
| **30** | 7 | **10** | 4 | 3882.492 | 23671.57 | |
| **31** | 33 | **51** | 4.1 | 3987.179 | 28427.34 | |
| **32** | 35 n.c. | | 4.2 | ? | ? | Missing? Check! |
| **33** | 25 | **39** | 4.3 | 4175.827 | 25554.87 | |
| **34** | 27 | **41** | 4.4 | 4271.555 | 26426.52 | |
| **35** | 17 | **26** | 4.5 | 4369.363 | 22921.30 | Changed in Run 71 |
| **36** | 19 | **29** | 4.6 | 4464.971 | 22196.59 | Changed in Run 71 |
| **37** | 9 | **12** | 4.7 | 4565.036 | 26027.27 | |
| **38** | 11 | **16** | 4.8 | 4663.911 | 26881.85 | |
| **39** | 1 | **1** | 4.9 | 4768.182 | 26482.76 | |
| **40** | 3 | **4** | 5 | 4858.547 | 29426.2 | |

### 2.1 LC# vs array location

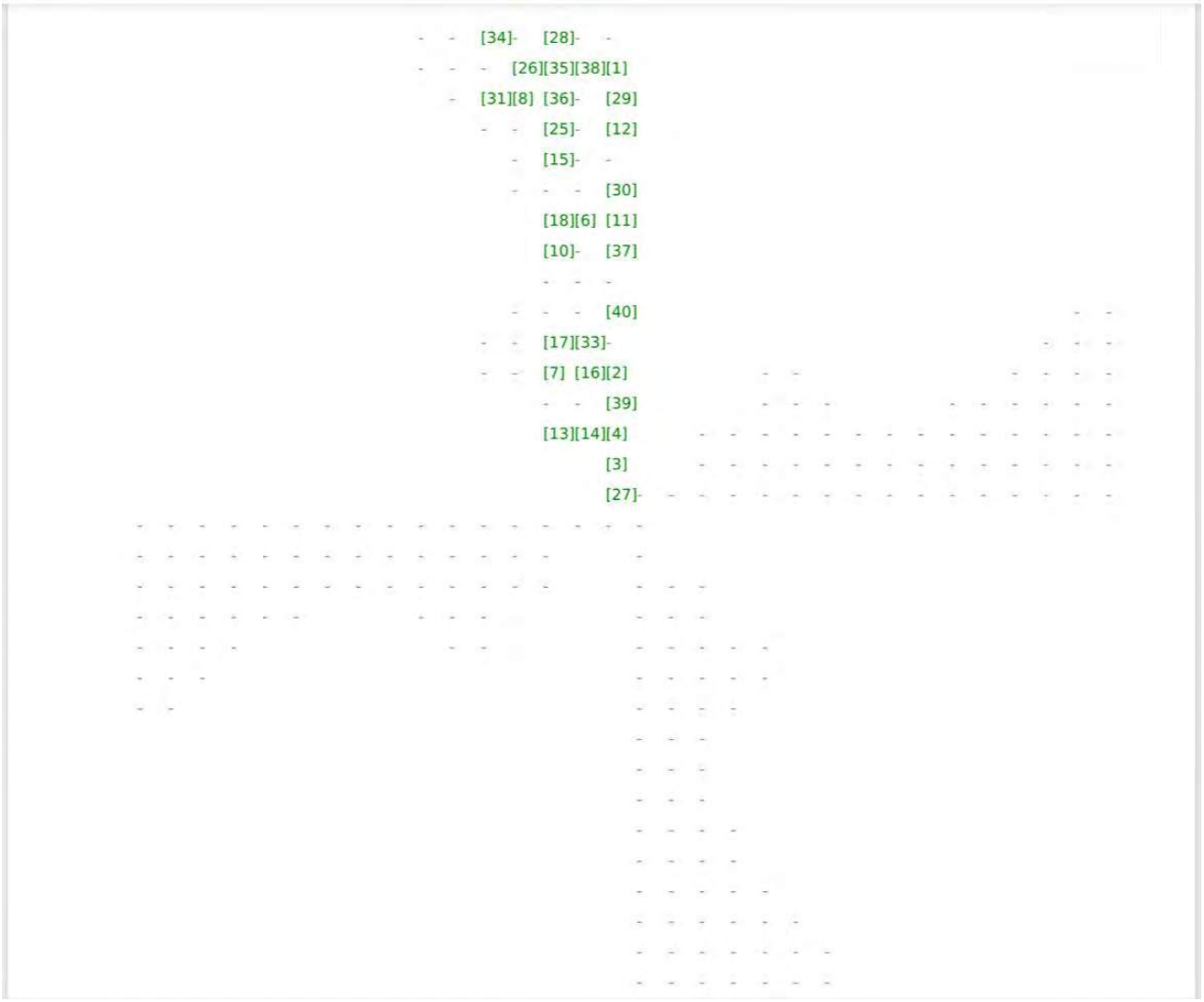



**Figure 2. [LC-filter #] plotted as location on the TES array (32x32 pixels), pad number can be found in table above.**

## 2.2 Designed wire bond scheme

Diagram of the wire-bonds planned for this setup:

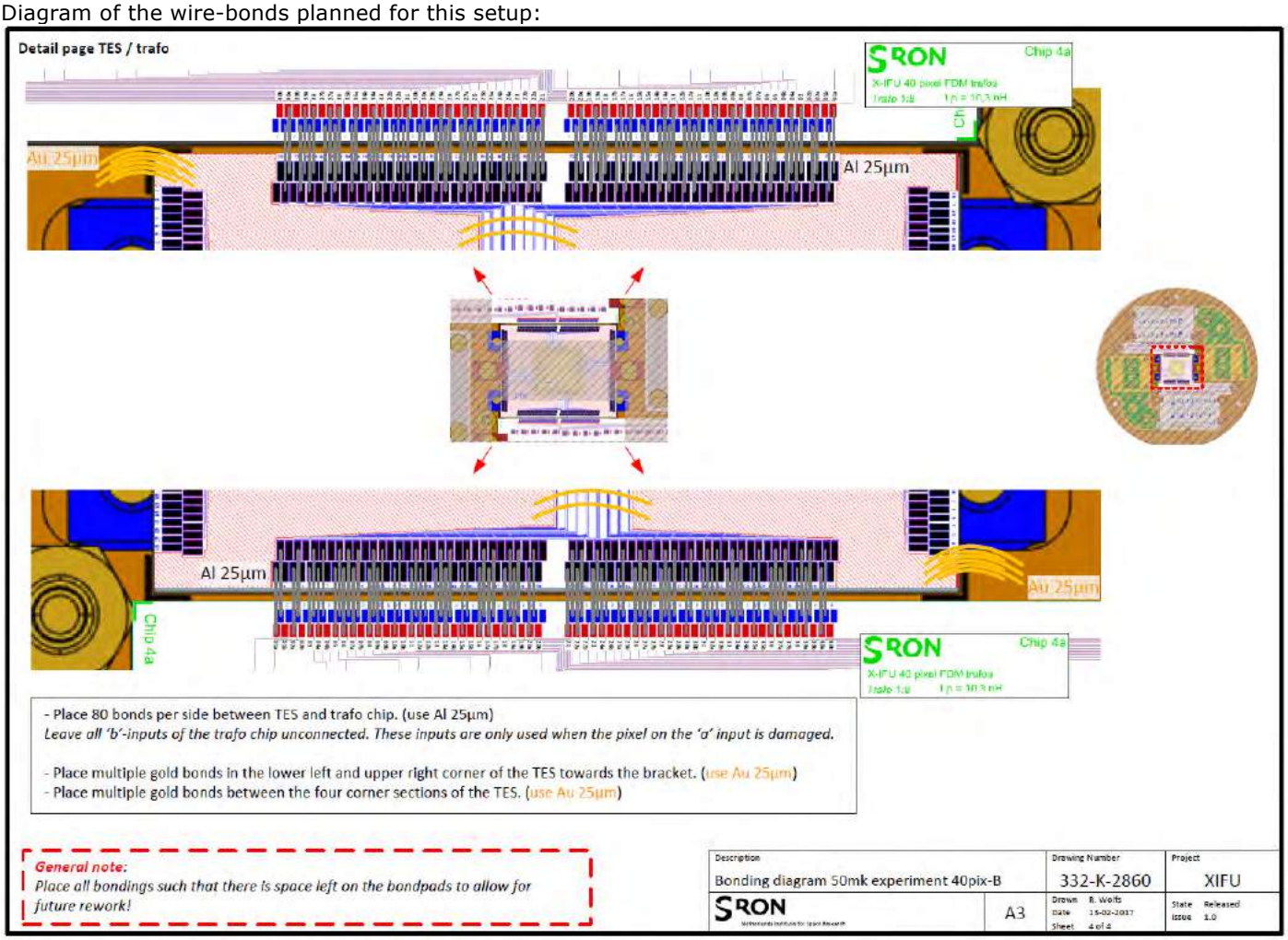



**Figure 3. Wirebond plan for large TES array 1 (GSFC-LA1).**

- Next run the Au-wirebonds between the left/right bottom/top gold thermalization planes have to be placed (not yet placed in this run)!

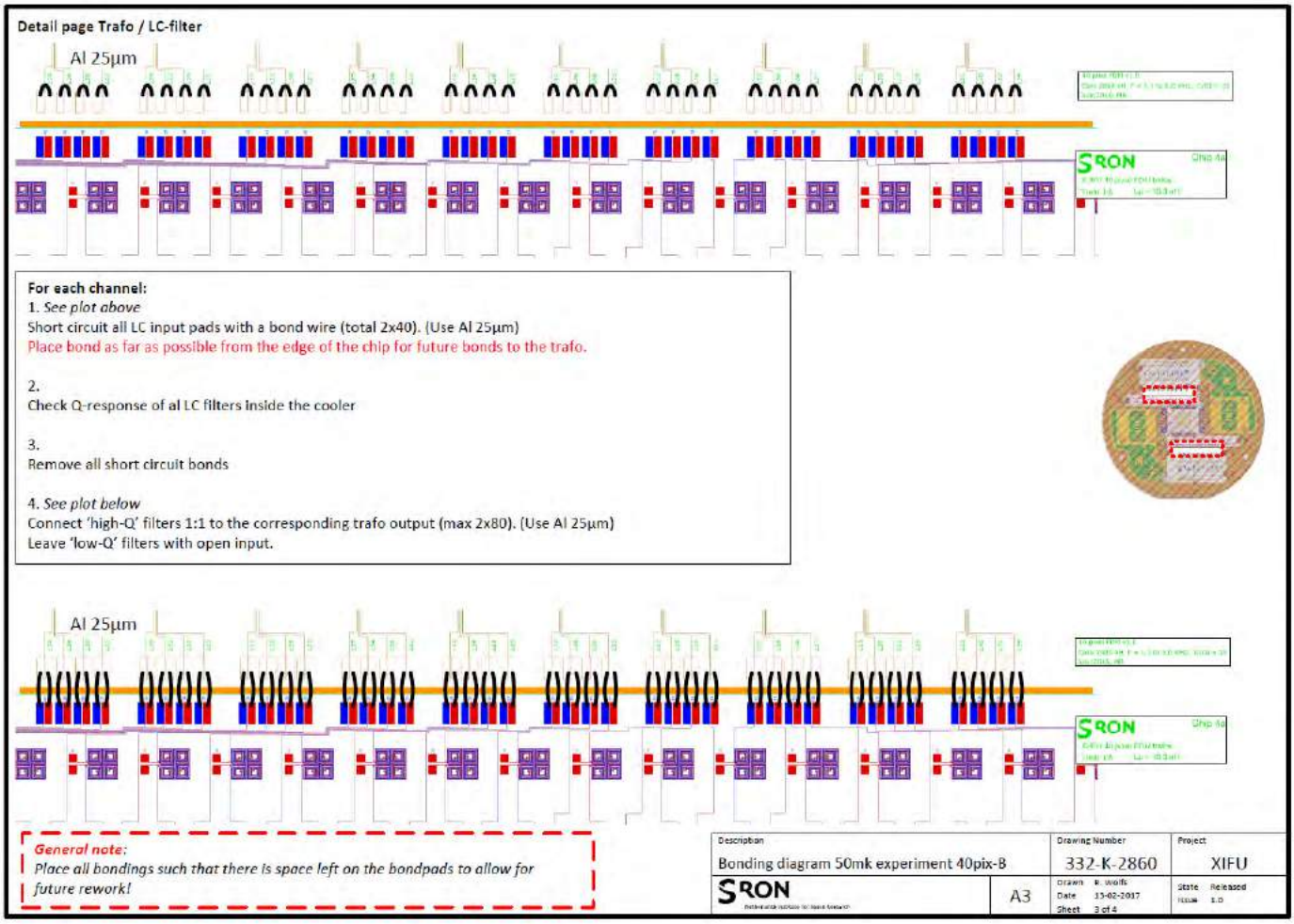



**Figure 4. Trafo - LC filter wirebond scheme, now 36/40 LC-filter have been connected to the transformer chip.**

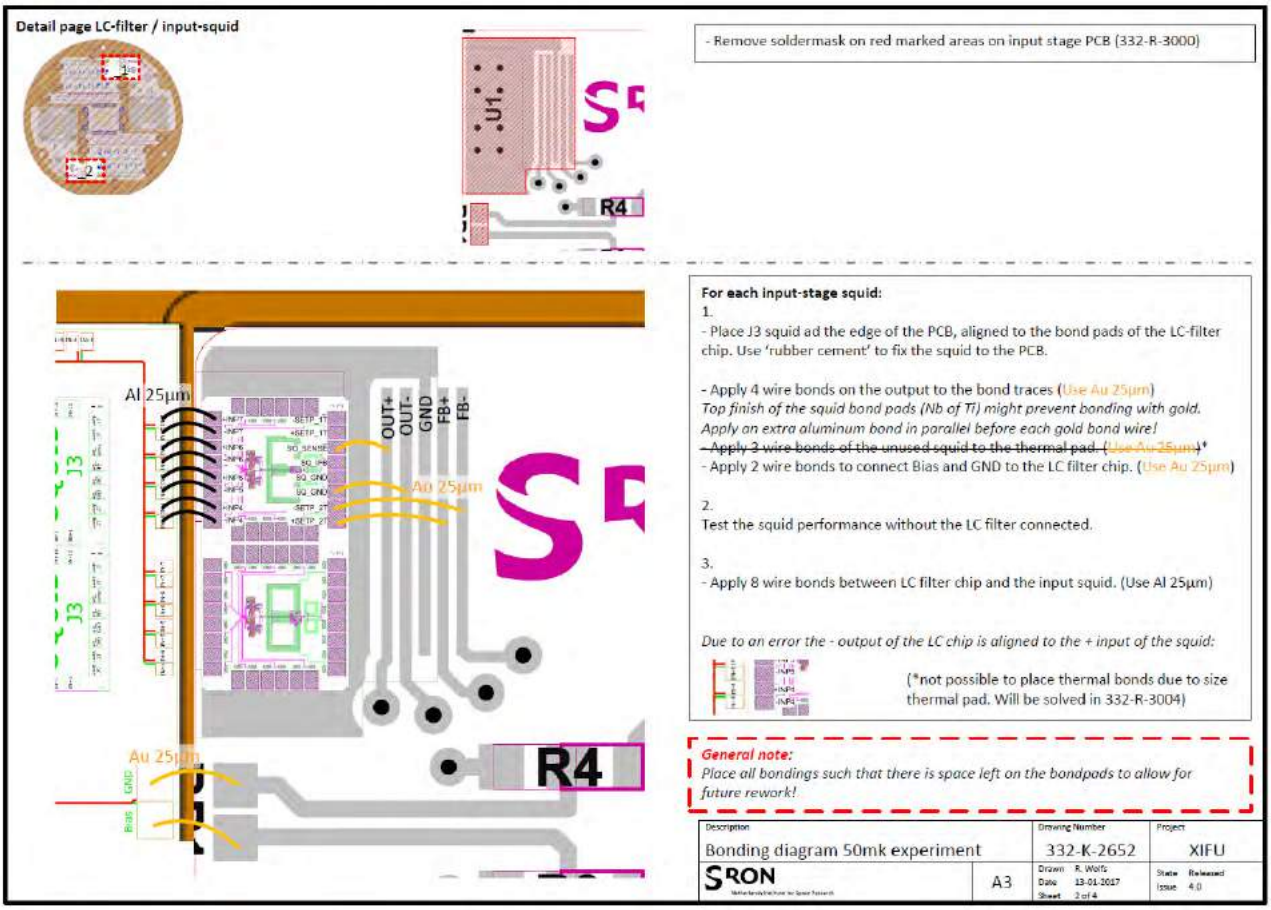



**Figure 5. 50mK bracket with input SQUID of FDM channel 1.**

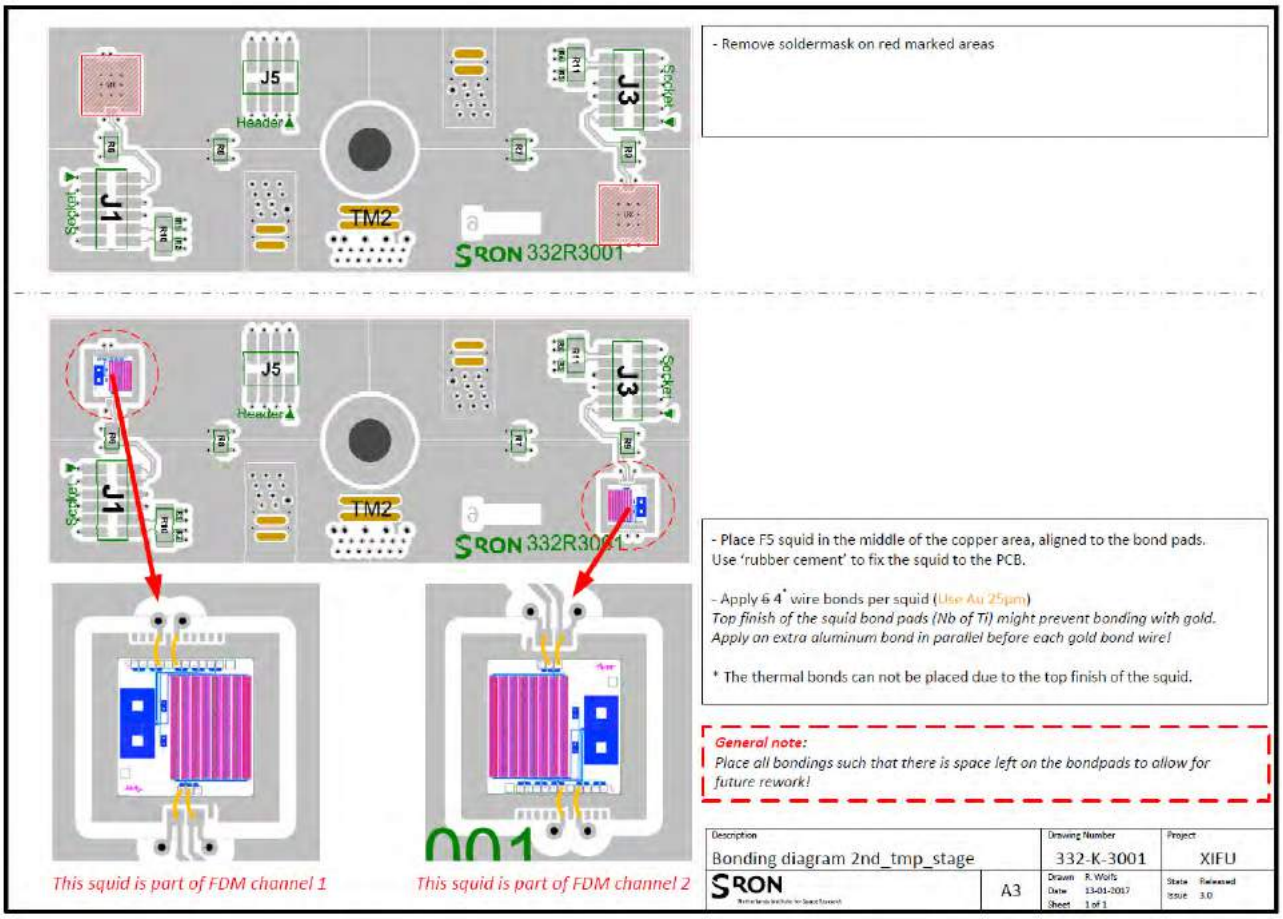



**Figure 6. 2nd temperature stage with output SQUID on FDM channel 1.**

Only one output SQUID (VTT F5 IEG#9) has been placed, the second channel is left empty for the coming cooldown runs.

On the current design of VTT F5 SQUIDs it is not possible to use Au-wire to bond to the thermalization pads and therefore have been left as is. The Bias and input coil lines have Au-wire bonds in parallel to the Al wire bonds for thermalizing the SQUID.

## 3 SQUIDs

Two tested SQUIDs have been connected in the first assembly, on channel 1 of the 40px FDM bracket (channel 2 is left empty). Both glued with rubber cement / photo glue, which is silicon based and is easily removable without solvents.

### 3.1 Input SQUID (VTT J3 on 50mK stage)

The Input SQUID has been placed on the PCB next to the LC-filter, and is connected to the LC-filter summing point.

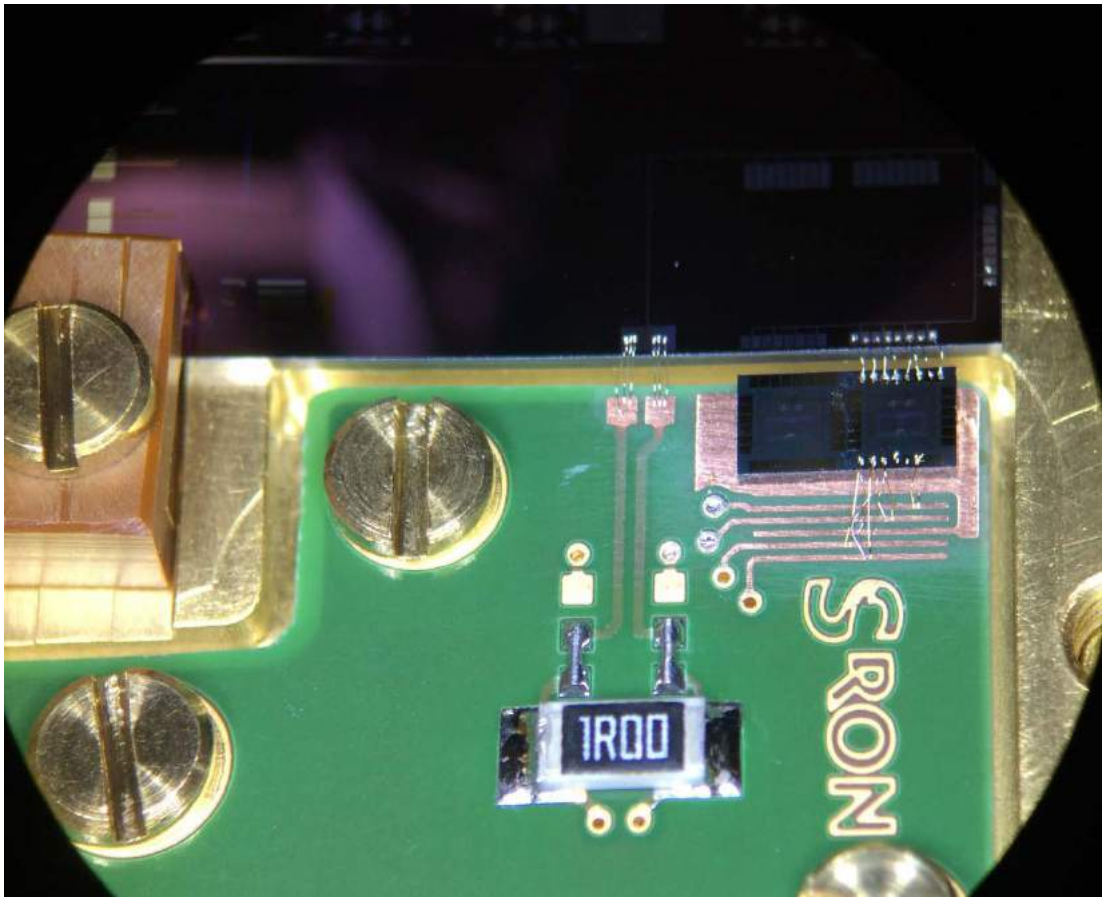



**Figure 7. "Input SQUID" VTT J3 connected to LC-chip and the AC-bias shunt resistance changed to 1.00 Ohm.**

| | | | | | | |
|---|---|---|---|---|---|---|
| **J3 array** | 6 SQUID array | retO | Utrecht - 40pxFDM | 03-01-2016 | see Kevin's email van 2016/6/29 \| update: best looking V-Phi from tested J3 SQUIDs, planned for 40pxFDM | tested in GFDM cooldown 77 |

### 3.2 Snubber circuit (LCrun66)

In order to damp/reduce the effect of high frequency oscillations from going into the Input SQUID, a low pass RC-filter was introduced (known as a ''snubber") at the LC-summing point.
This filter consists of a 5Ohm resistance and 1nF capacitor (with 6.8pF in parallel for high frequencies) which sits in parallel with the input coil of the Input SQUID.

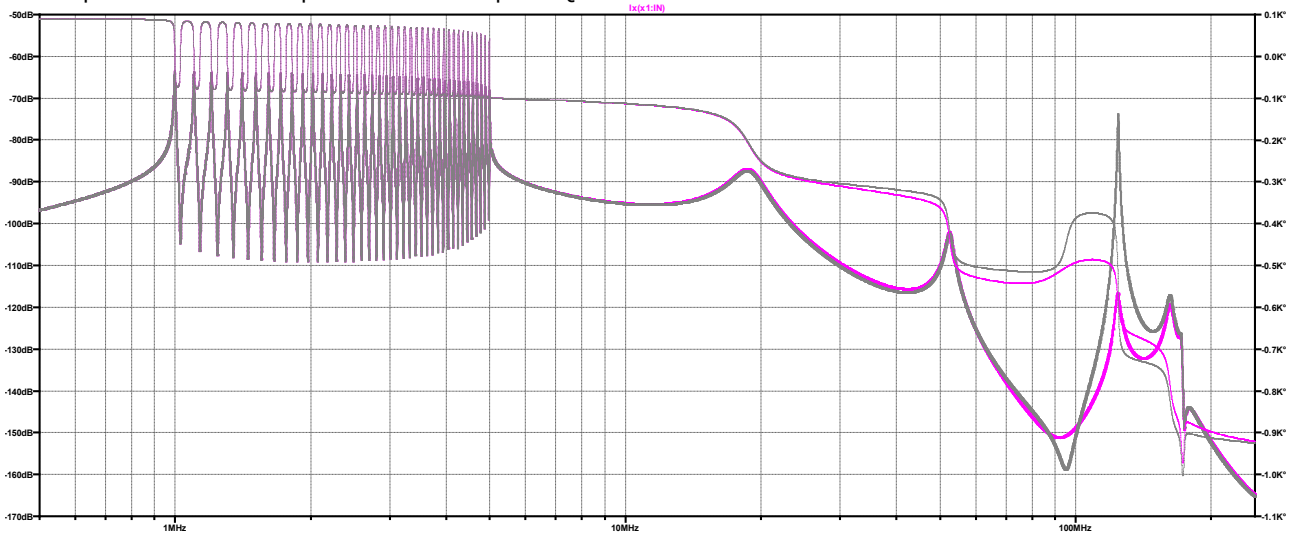



**Figure 8. Simulated circuit, plotted current at Input SQUID coil (grey without snubber, magenta with snubber). LTSpice Model by Ad Nieuwenhuizen.**

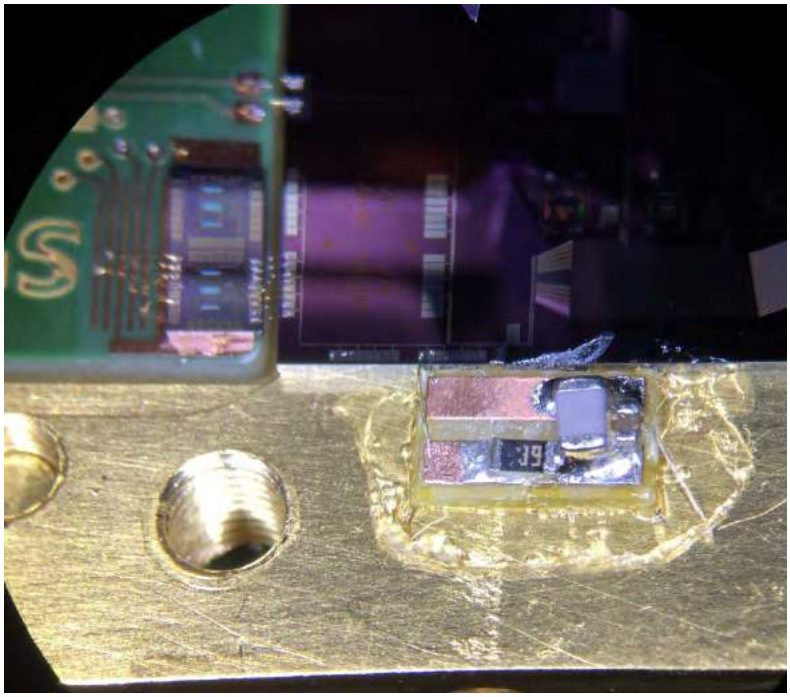


**Figure 9. Snubber circuit as implemented on 40 pixel A setup in LC run 66 (11-10-2017).**

This had the desired effect of damping the oscillations in the circuit, making both flanks workable again!

### 3.3 Output SQUID (VTT F5 on 2nd stage)

VTT F5 SQUID on channel 1 of the 40px FDM 2nd stage PCB. Connected with Al and Au wirebonds for thermalization. The thermalization pad cannot be bonded to with Au on this SQUID, the material is not compatible (we have tried many times before).

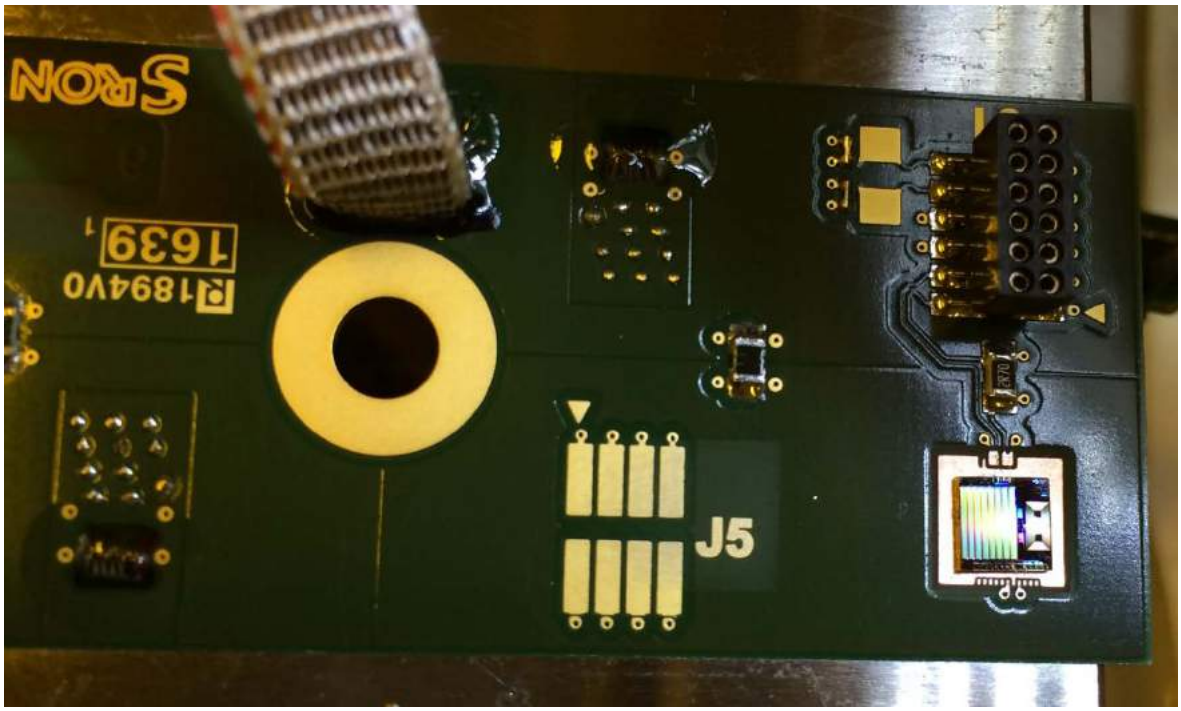



**Figure 10. 2nd stage PCB with "Output SQUID" glued to PCB and wire-bonded with Au-wires to channel #1.**

| | | | | | | |
|---|---|---|---|---|---|---|
| **F5 array** | 184x4 SQUID array | IEG#9 | Utrecht - 40pxFDM | 03-01-2016 | low IC F5 chips \| Showed little/no distortion in V/Phi curve when tested at 50mK in GFDM setup | tested in GFDM cooldown 77 |

For run 65 we re-did the wire bonding of the Output SQUID, as two of the connected wires had come loose. This likely was the cause of not working Output SQUID flux offset, the V/Phi scan gave a flat line.

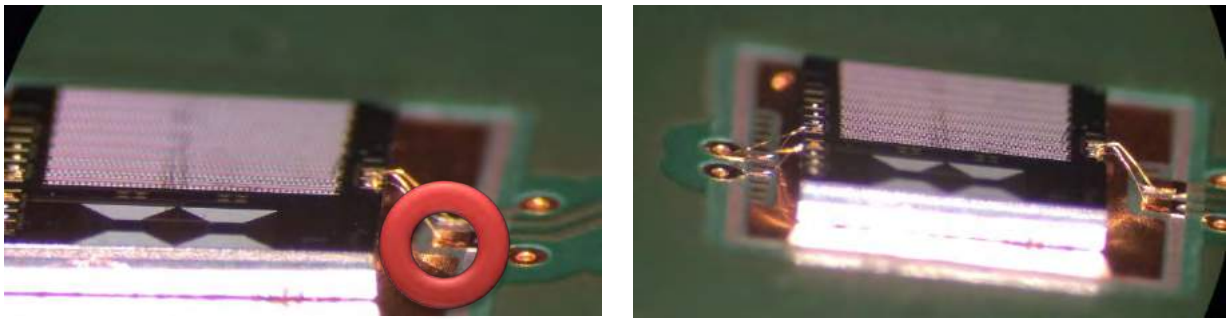


**Figure 11a, 8b. Output SQUID as of LC run 63 / 64, before reparation action.**

Here the wire that was only making light contact, not physically bonded any more, to the copper PCB pad. The faulty wire was removed from the SQUID, after which a new connection was made between PCB and Output SQUID input coil.

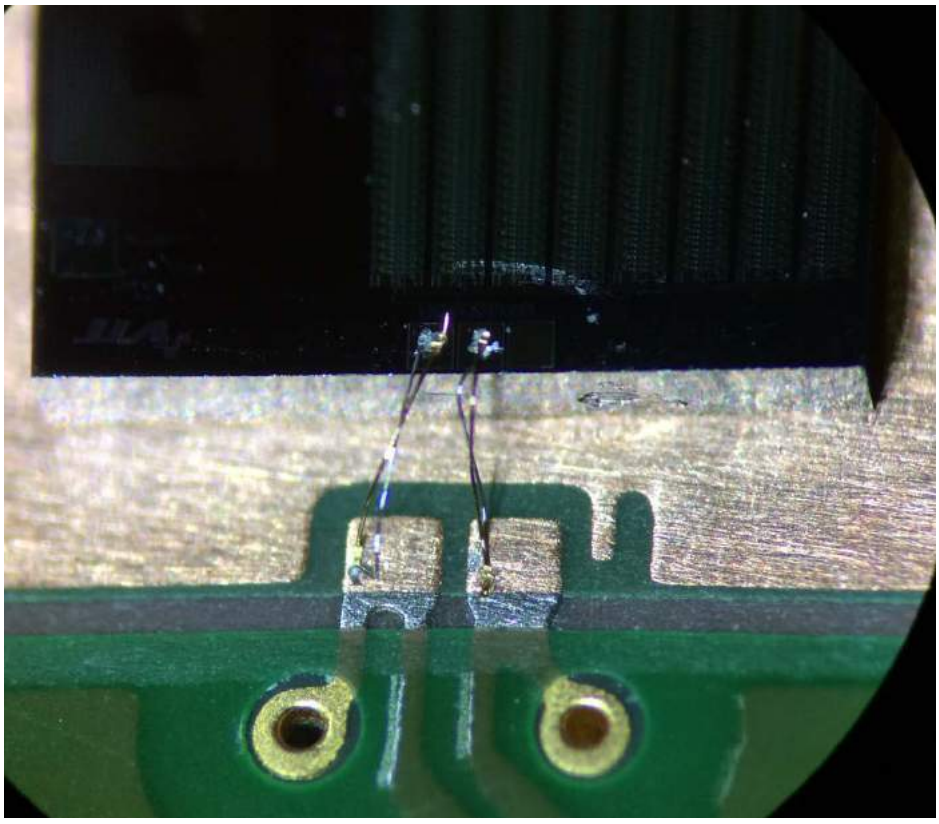


**Figure 12. Output SQUID as of LC run 65, after reparation action.**

After repairing the faulty connection by placing an Al-wire and Au-wire in parallel.
The newly placed wires were all tested by pulling lightly on it with the tip of the Westbond wire-bonding machine, all connections passed as they did not move much or got loose.

## 4 LC-filters (wafer LC17-1 chip 1b, 40 usable channels)

Only the LC filter of 40px FDM channel 1 has been placed on the 50mK bracket. Test report of this chip:

| | # OK | Remarks |
|---|---|---|
| TES input strip-line | 40 | MΩ regime. |
| Bias summing point | | 8.8 MΩ |
| Squid summing point | | O.L. MΩ |
| Capacitors | 40 | |
| Bias capacitors | 40 | |
| Coils | 39 | From optical inspection. Not electrically measured. |

Chip can be used for 40 or 39 pixels (assuming small resonance frequency shift of channel 21).

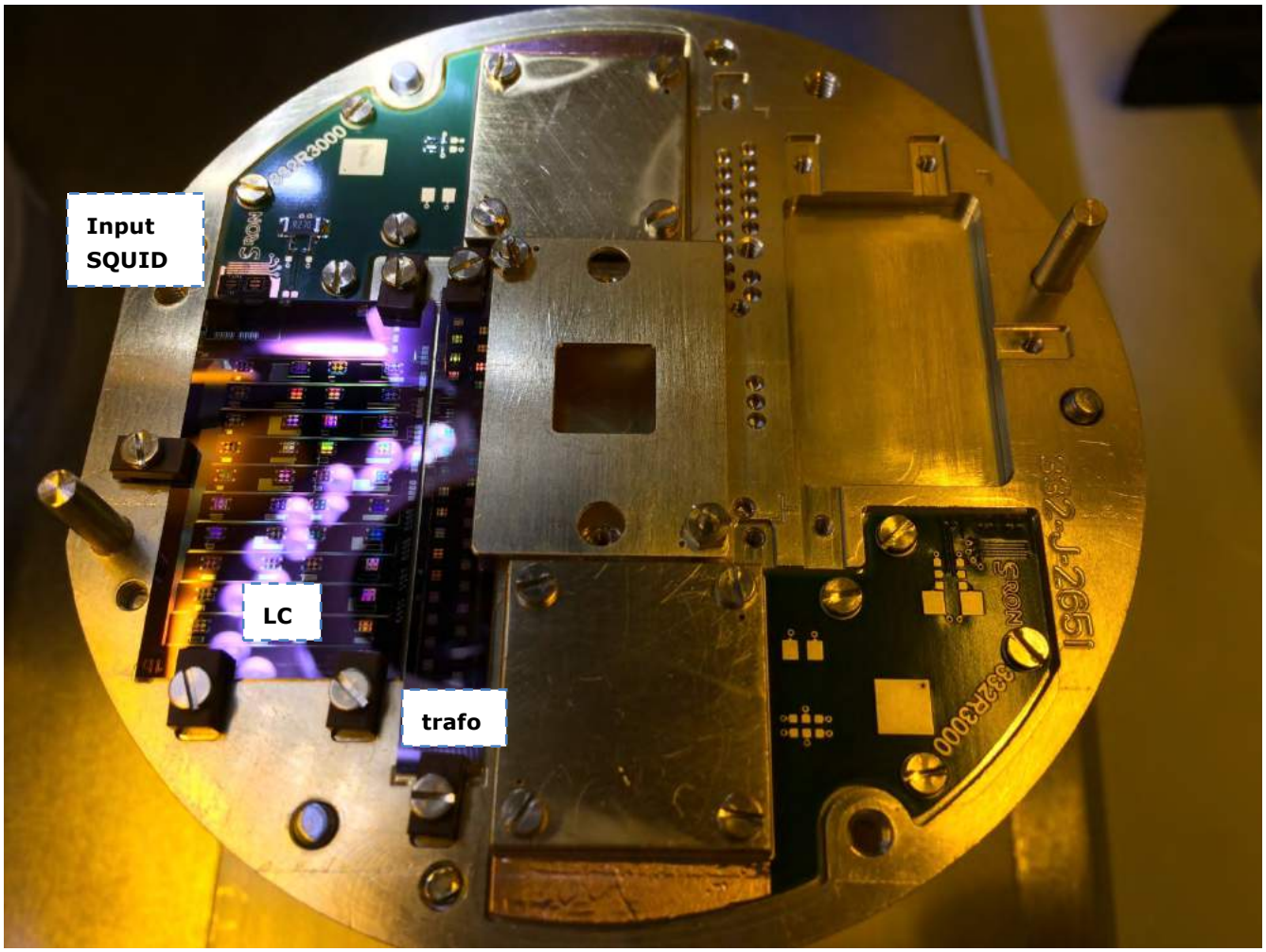



**Figure 13. 50mK bracket with FDM chips clamped or glued to the bracket/PCB.**

All LC's except #21 have already been shorted at the TES side. The J3 SQUID is now connected to the summing point of the LC filter chip with several parallel wire-bond connections.

## 5 Transformer chip (wafer SC10-3 chip 4a)

As of LC run 69 a previously tested transformer chip has been placed back, with 1:8 ratio coils (primary coil inductance designed to 10.3nH still, secondary coil differs in turns), namely chip 4a from the same wafer SC10-3.

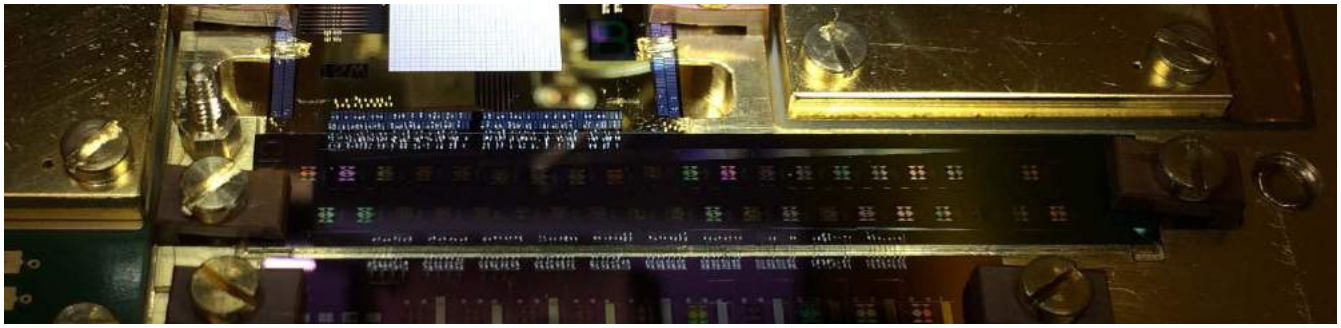


**Figure 14. Trafo from run 65 re-introduced.**

This chip had a yield of 40/40 transformers. During coupling factor run, only trafo 37 was not shorted properly.

No changes have been made to the pixel layout/connections. With the 1:5 ratio transformer we had oscillating pulses (TES too fast for the feedback bandwidth).

## 6 GSFC TES array

Introduced in cooldown 5, or LC run 63. All available LC resonators have been connected to a TES, preferably one that was tested at GSFC before.

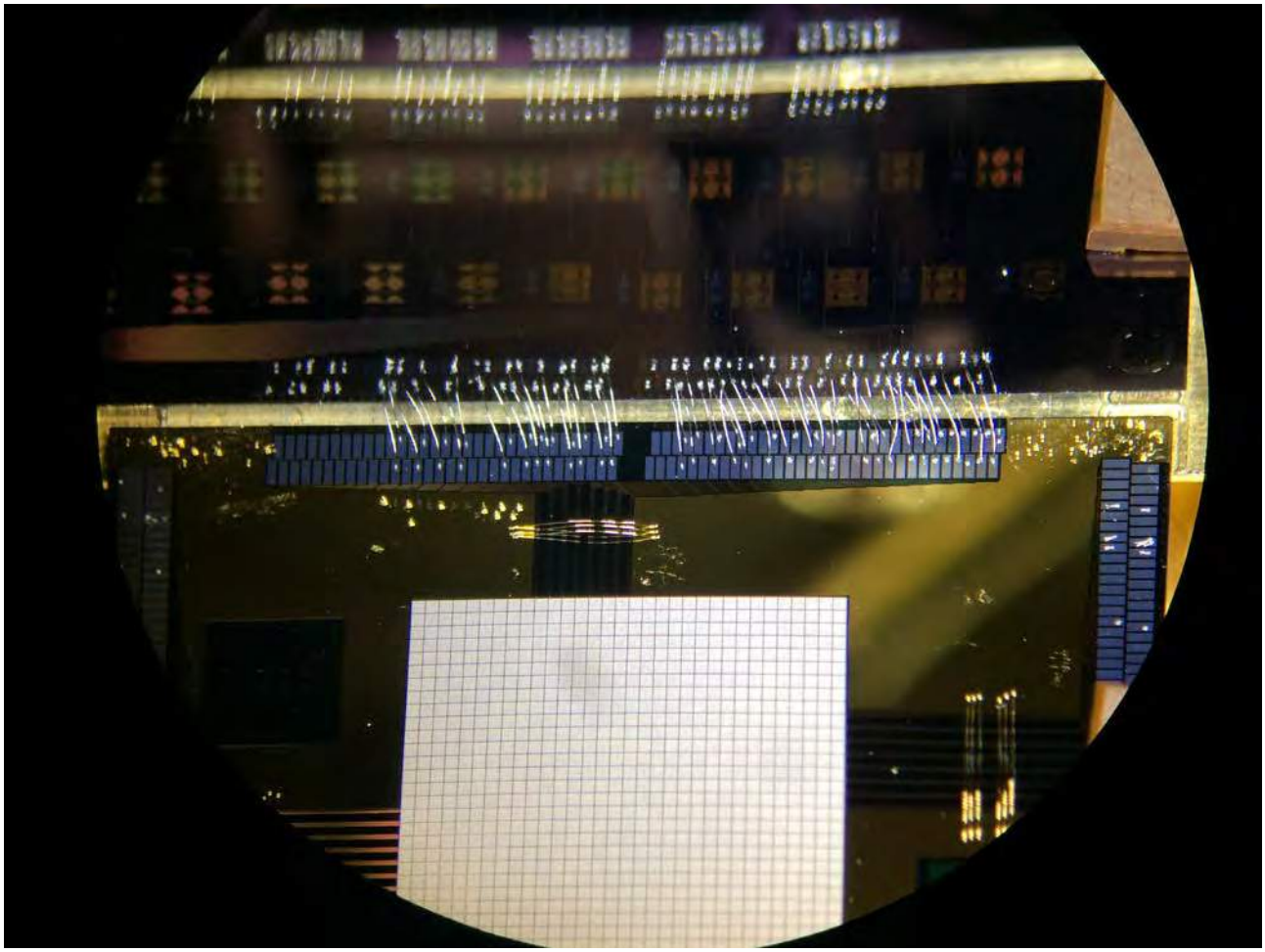


**Figure 15. GSFC LA1 mounted on 40 pixel FDM - A setup and connected with Al-wire bonds to the transformer chip. In Run 71 the array was rotated and Quadrant 1 connected instead of 3.**

Collimator plate was covered by Cu-tape until Run 71, now all pixels should be illumined with X-rays again.

### 6.1 Thermalization Au-wire bonds

To thermalize the TES array, only the plastic clamps won't be enough, so several gold wirebonds have been connected from the bracket surface to the thermalization layer on the chip.

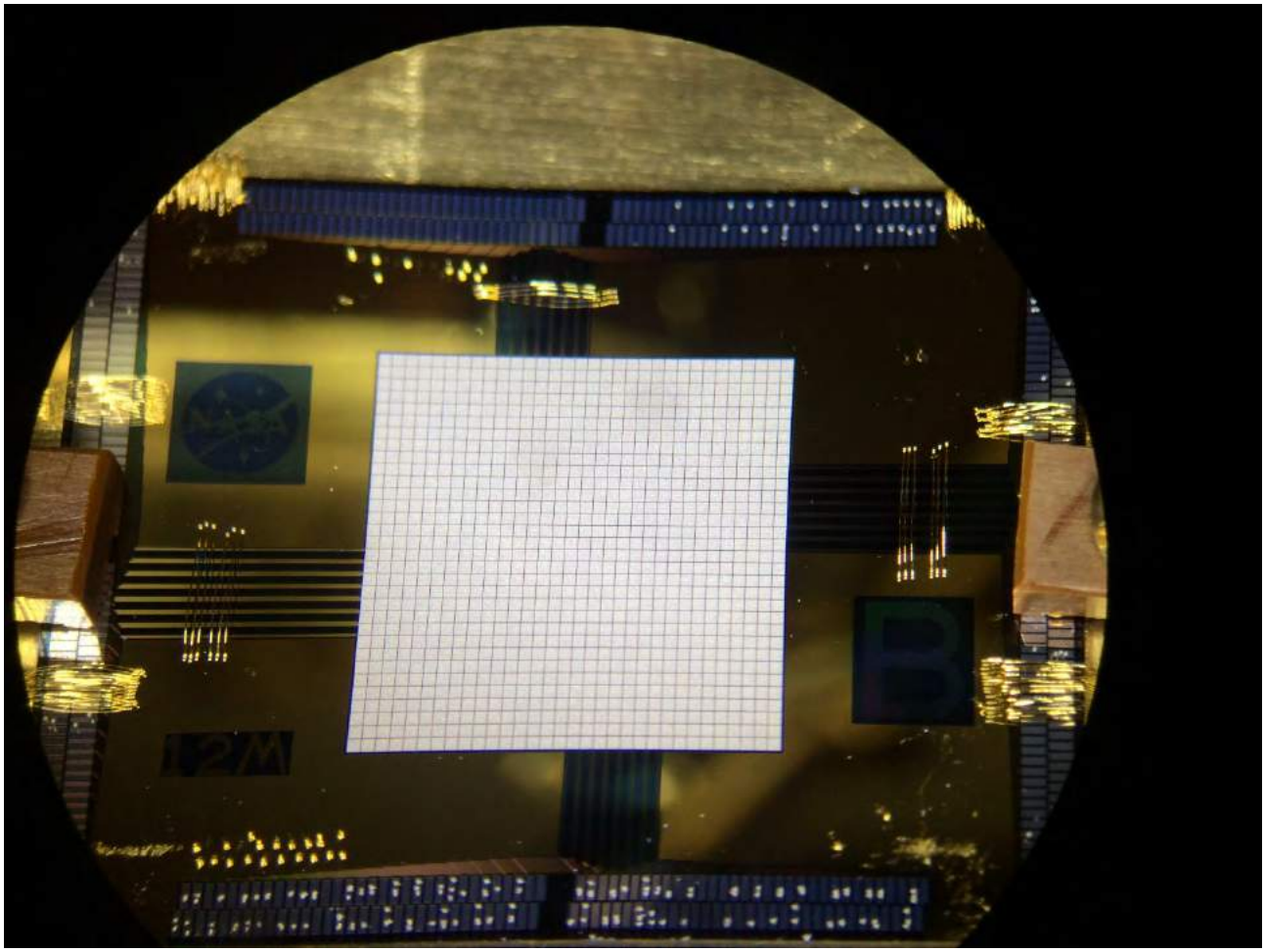


**Figure 16. Au-wire bonds (extra added) on GSFC LA1 TES array, as connected in Cooldown 11 / LC run 69.**

In Run 71 the Au-wire bonds had to be remade, as the array was rotated 180 degrees to connect quadrant 1.

## 7 X-ray Source #4

From LC-run 65 we have mounted X-ray source #4 (used on XFDM-Probe before) on the 50mK bracket/cap.

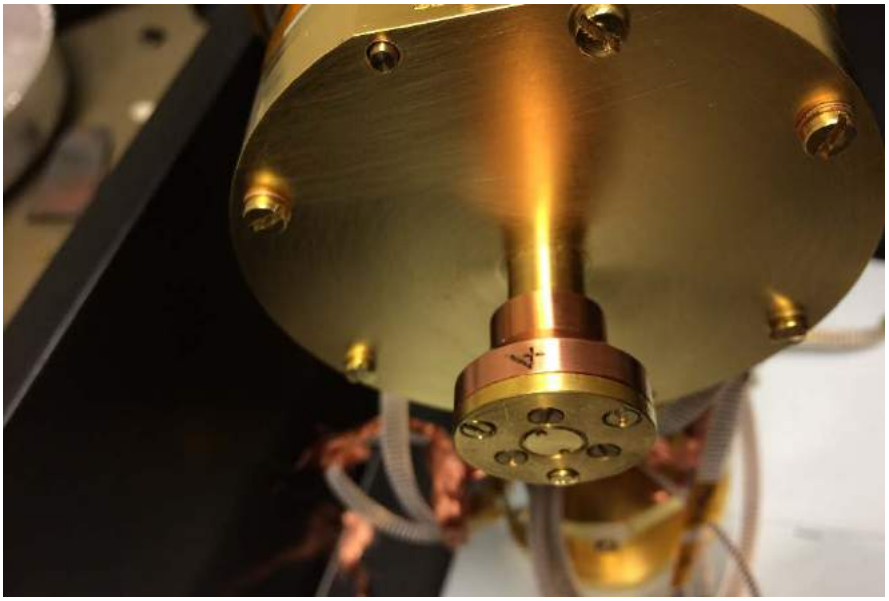


**Figure 17. X-ray source mounted on 40 pixel A, picture taken before LC run 67, 14-11-2017.**

## 8 Kevlar suspension (LCrun67)

In LC run 67 we first introduced the Kevlar suspension on the 40 pixel A setup, a length of 50.0cm single bundle (not woven) of Kevlar wire was clamped between the white plastic wire guides. The lower part of the setup was very stable, not dangling when the cooler was pushed. Also a quick test with the Pulse tube ON gave an idea of the damping effect by the Kevlar, which was similar to that of the XFDM setup.

**Figure 18. Kevlar wire introduced in LCrun67, picture from 14-11-2017.**

**Figure 19. Black marked section to define 50cm length, 2 spare Kevlar wires are marked too.**

To prevent dangling loom headers, we taped the looms to the bulky 'tombstone' bracket of the setup.

## 9 Pictures

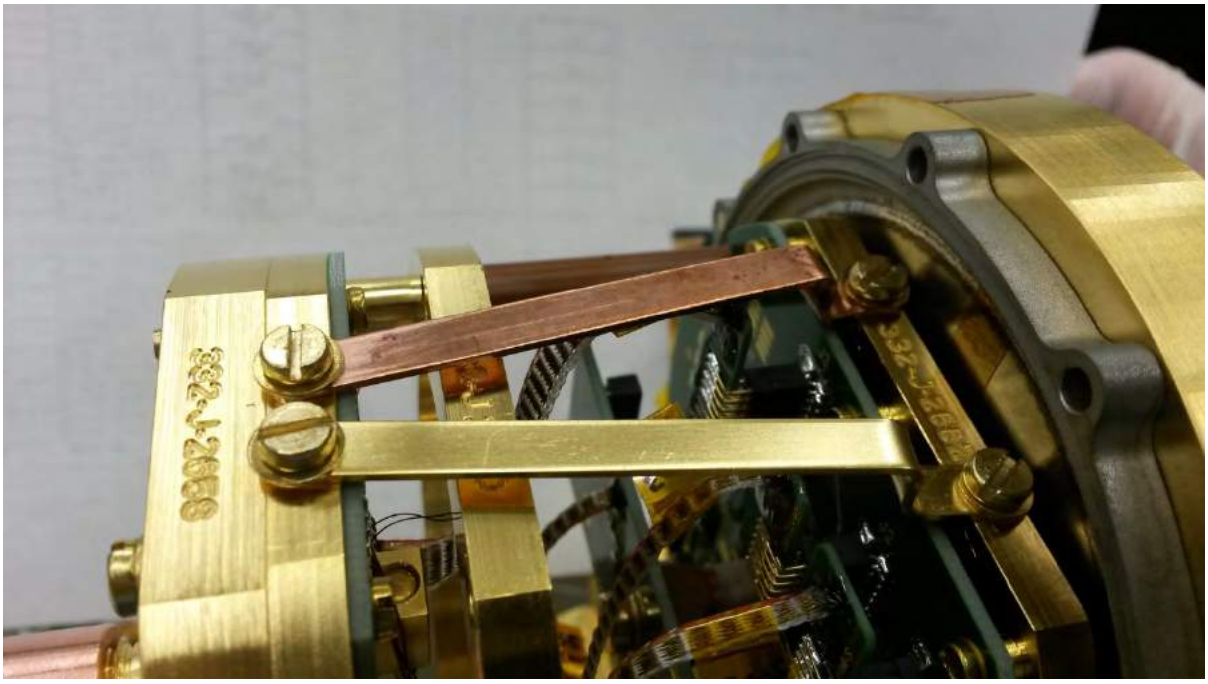


**Figure 20. Extra Cu-thermal connection from the 50mK stage to the base plate / ''tombstone''.**

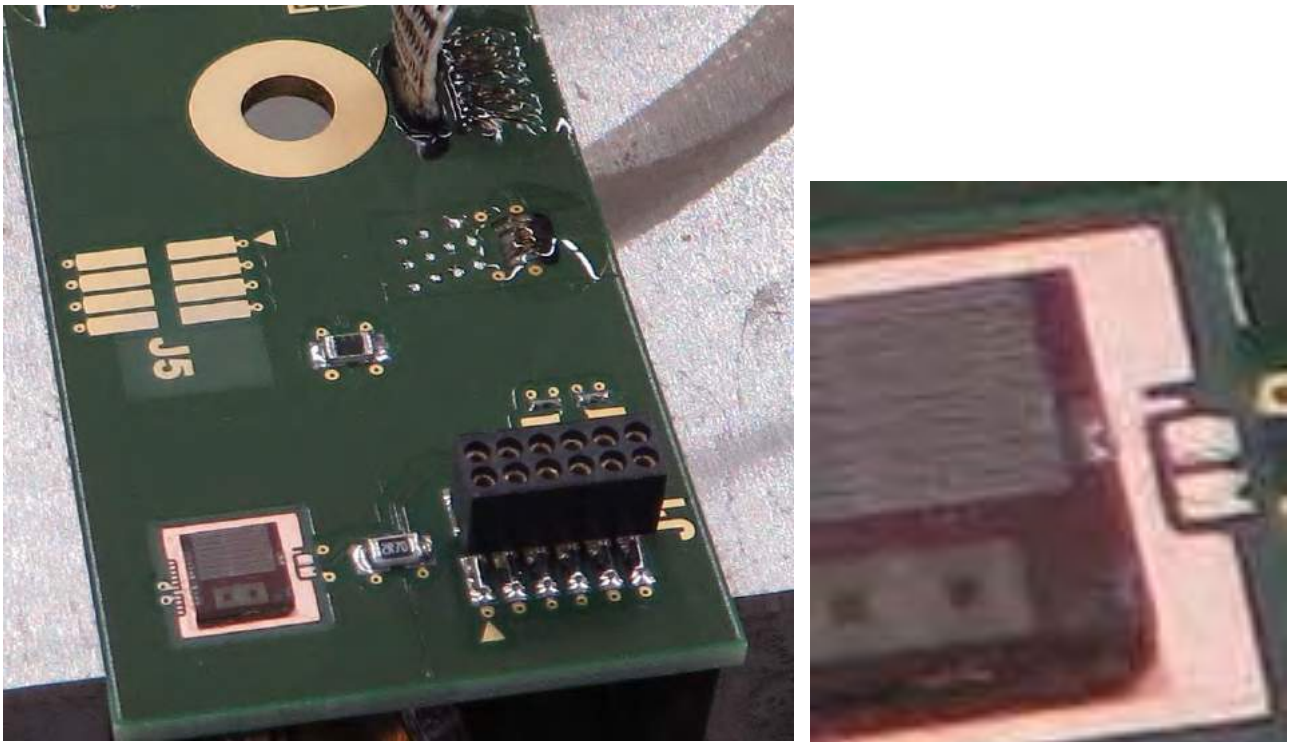



**Figure 21. Output SQUID (VTT F5) as it was during first assembly of the setup, already with handling mark/surface scratch at the input pads side.**

**Figure 22. 40 pixel experiment location in SRON Utrecht LC-cooler, during Run 60.**

## Appendix 5
## EFDM setup overview

SRON
Netherlands Institute for Space Research

# E-FDM LC-run 69

Date: 2018-4-5
By: Kevin Ravensberg
V0.2 – edited Snubber resistance value to 5Ohm (2x10Ohm parallel!)

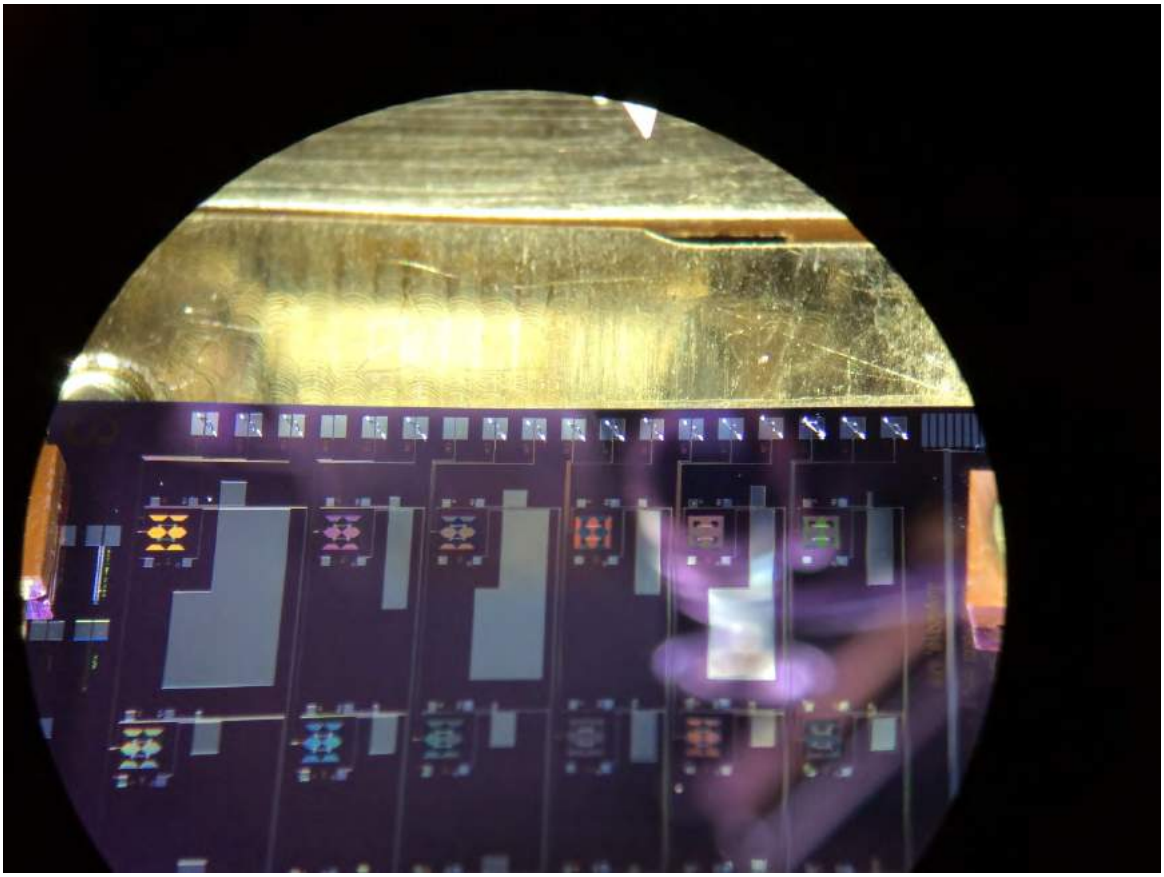


*Figure 1. E-FDM with LC-filter chip 3 (wafer LC18-x) with shorted LC-filters at trafo side.*

## Contents

## Introduction

In this document an overview is given of the SQUIDs used in the E-FDM setup (previously known as the G-FDM / SQUID test setup used in Groningen), this 18-channel FDM setup will primarily be used to debug the SQUID read-out chain and tests requested by our Engineering Group (EG).
An overview of the history of this setup can be found on the Owncloud server of SRON at this location: https://owncloud.sron.nl/owncloud/index.php/s/NVt3BwfwTEGIIxv

## Setup overview

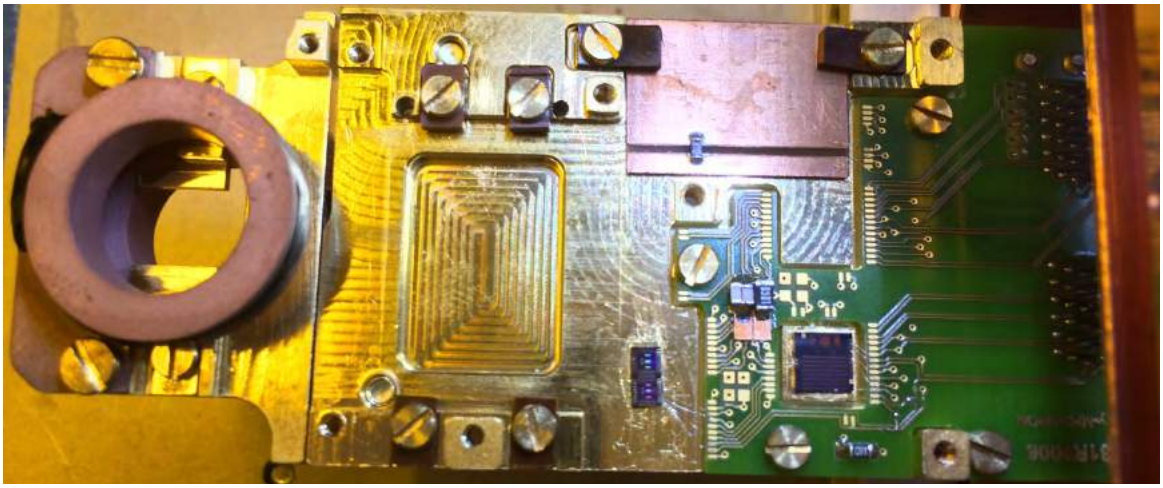


*Figure 2. Bracket of E-FDM with newly mounted magnetic field coil and TES array holder (on the left).*

A noise level was calculated in LC-run 66 of around **~5pA/sqrt(Hz)**, by taking the signal to noise ratio of a calibration tone.

**SQUIDs:**

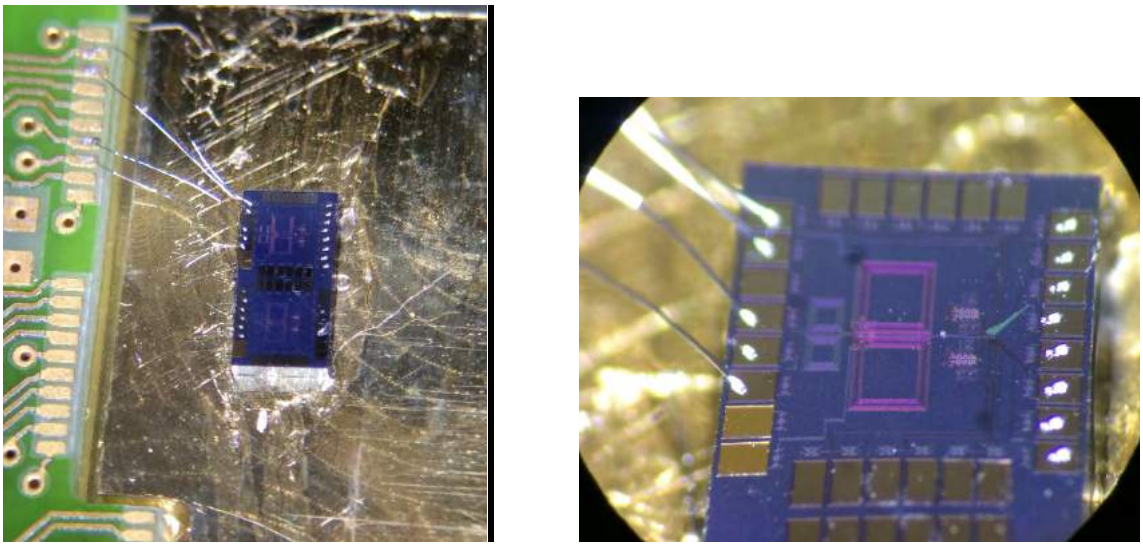


*Figure 3. J3 SQUID as used on the E-FDM setup in Run 67.*

VTT F5 'c' or p (ret.1) and VTT J3 (ret V wafer #28) are used since the last runs in Groningen.
As there is no LC-chip mounted, the input coil of the Input SQUID is open. Only the noise levels and DC characterization have been measured the previous run.

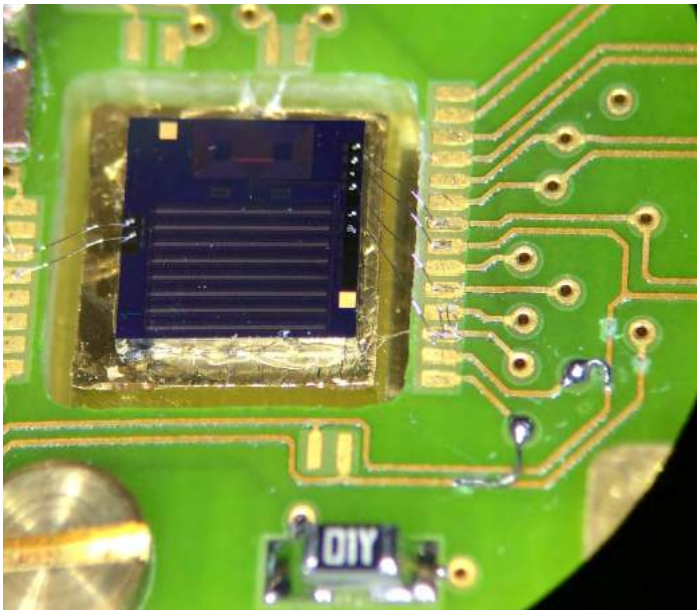



*Figure 4. Output SQUID (VTT F5) as used on the E-FDM setup in Run 67.*

**Snubber chip**

RC-filter (snubber) between Output SQUID input coil and Input SQUID signal line has been implemented.

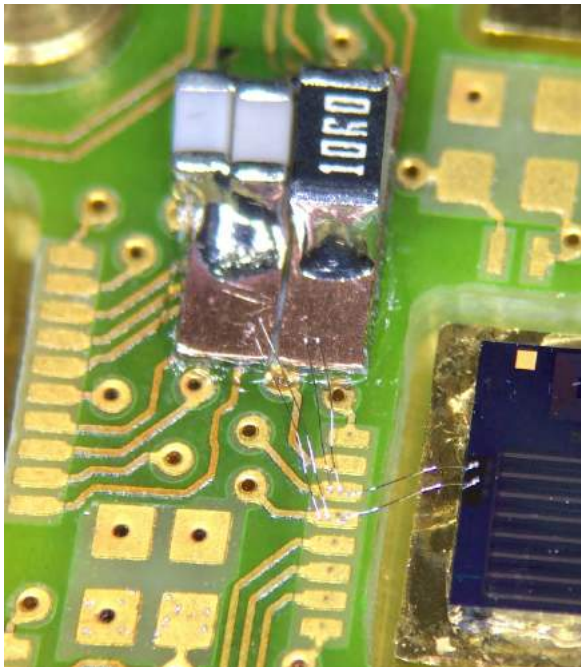



*Figure 5. Snubber RC circuit as implemented in LCrun67, with 5Ohm (*2x10Ohm ||) resistance and 470pF capacitor (6.8pF in parallel).*

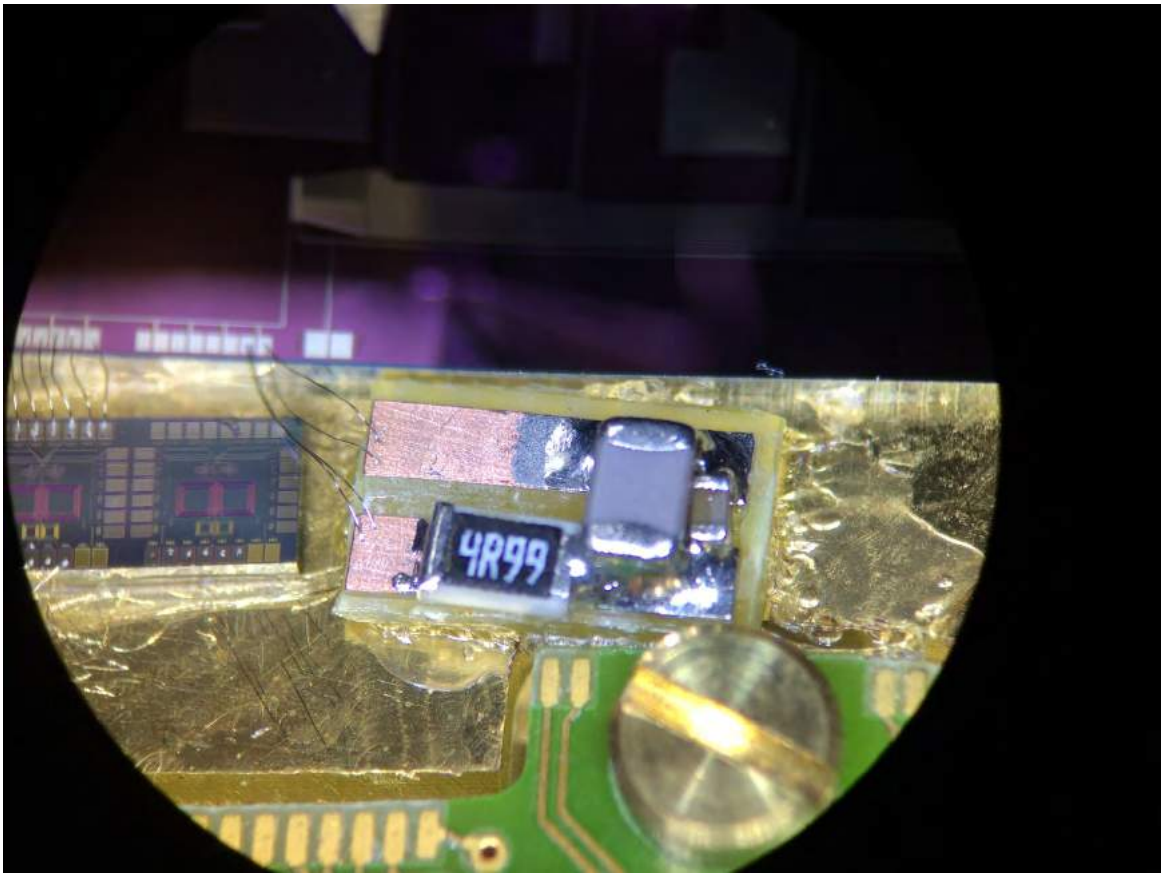



*Figure 6. Snubber at input coil of Input SQUID.*

**LC-filter chip**

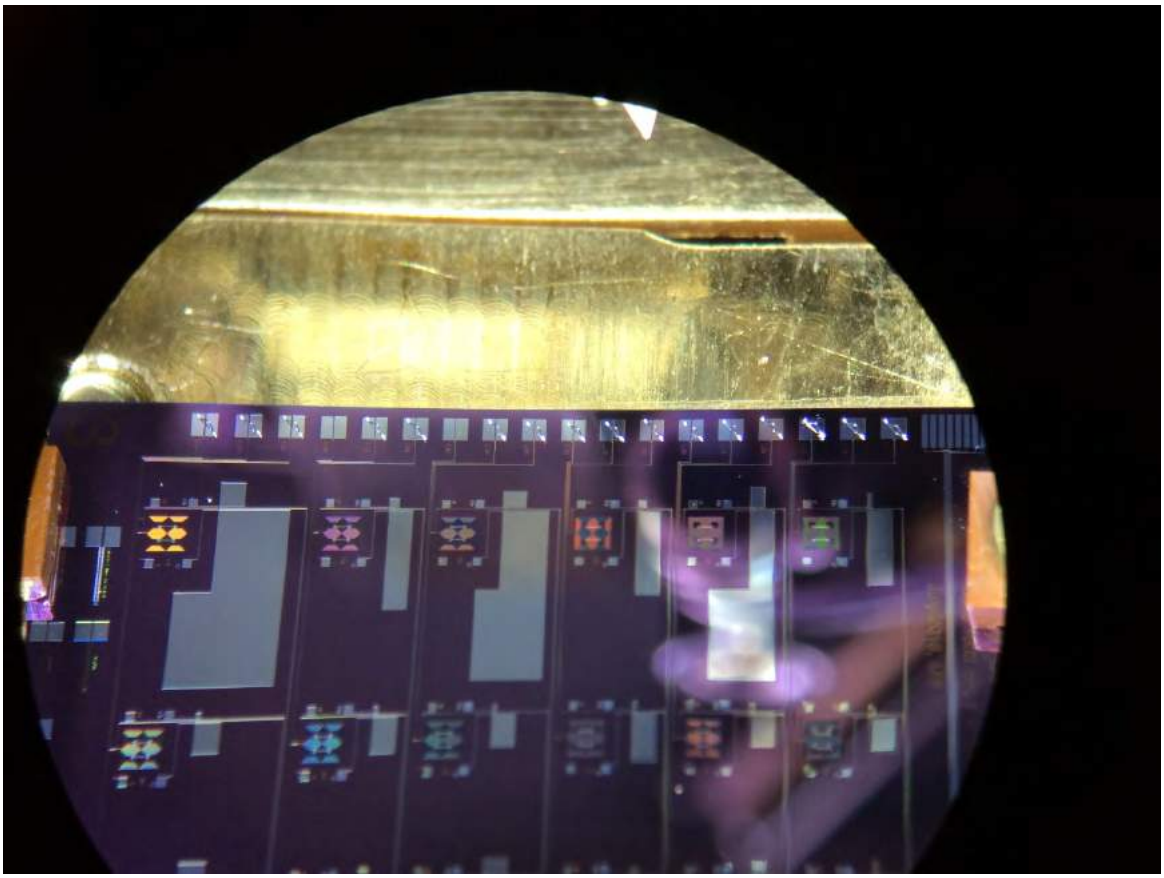
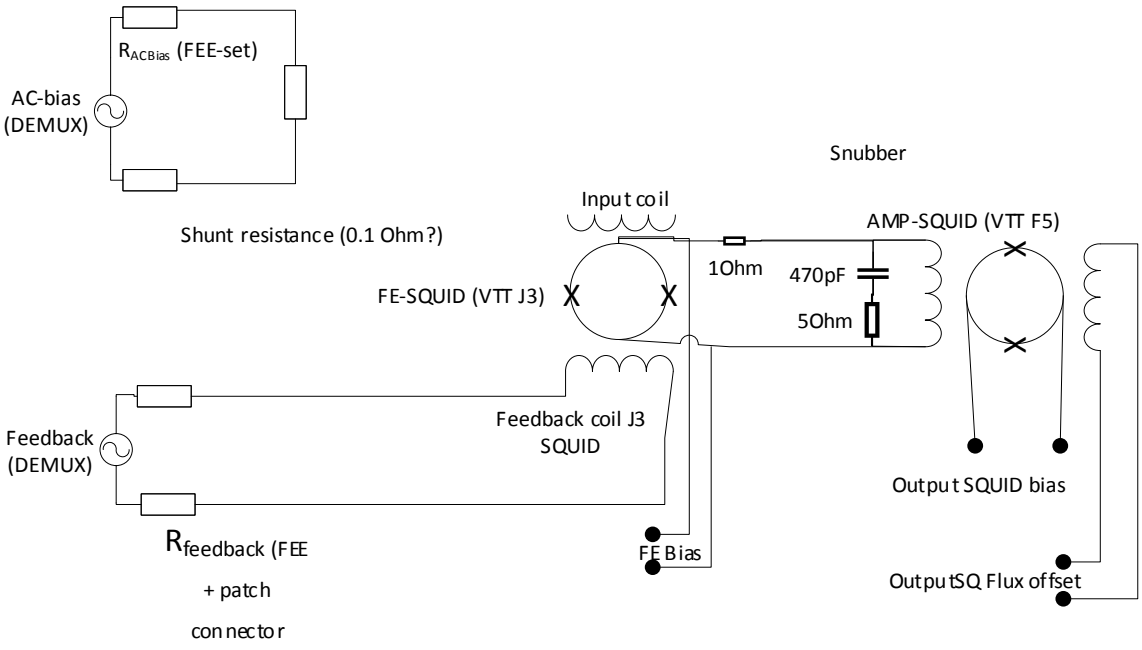


*Figure 7. Wafer: LC 18-x (unknown, 2/3), Chip 3 with 1/25 Cbias/C ratio.*

Chip from batch LC18 was introduced, with high Q-factors to investigate the effect on the SQUID.

## Schematic overview




Schematic overview of setup during LC run 67, FDM setup without LC-filters or TES's.

## Measurement results

Both a DC characterization and Noise scan as a function of SQUID bias / flux combinations have been taken. First results indicated that there is an extra oscillating line around ~14MHz which is badly disturbing the read-out system.
Data without snubber can be found here: /stage/ltsboldat5/E-FDM/LCrun66_3

FLL – mode VI of Input SQUID:

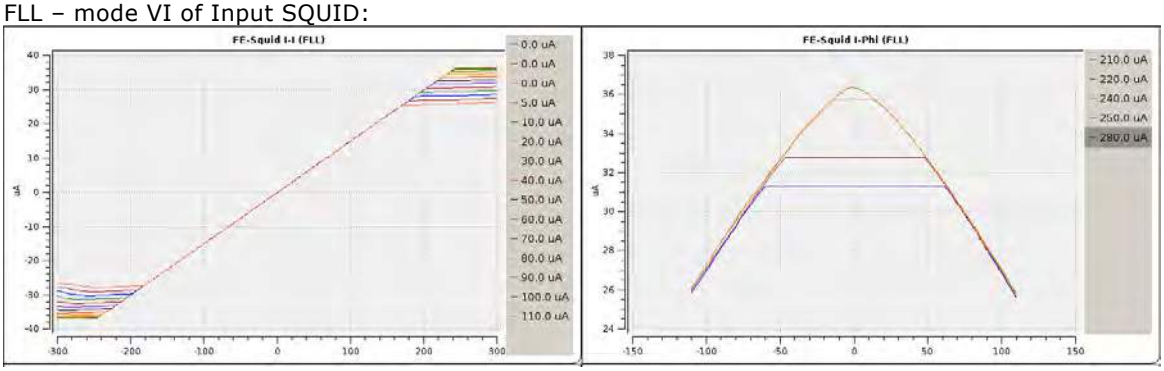



*Figure 8. Flux locked loop operation of the Output SQUID, scanned VI and VPhi of Input SQUID in Run 67.*

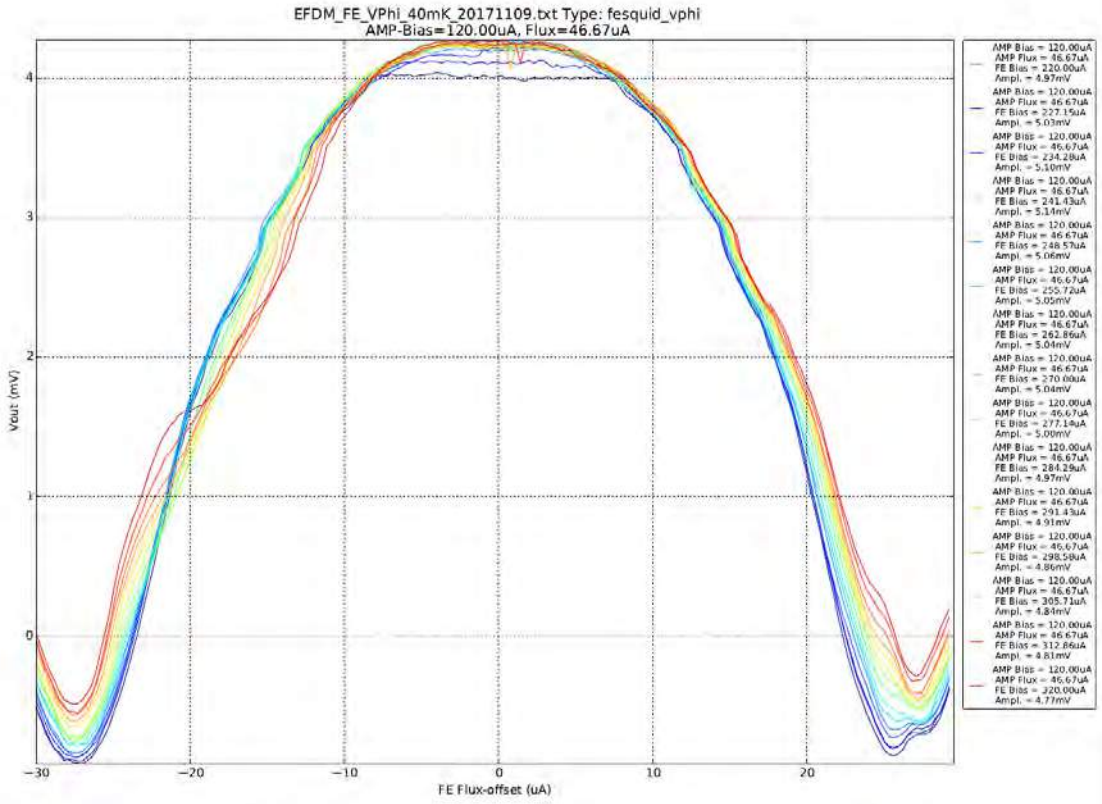



*Figure 9. Input SQUID V/Phi curve, from LC run 66 without snubber or SC-shielding.*

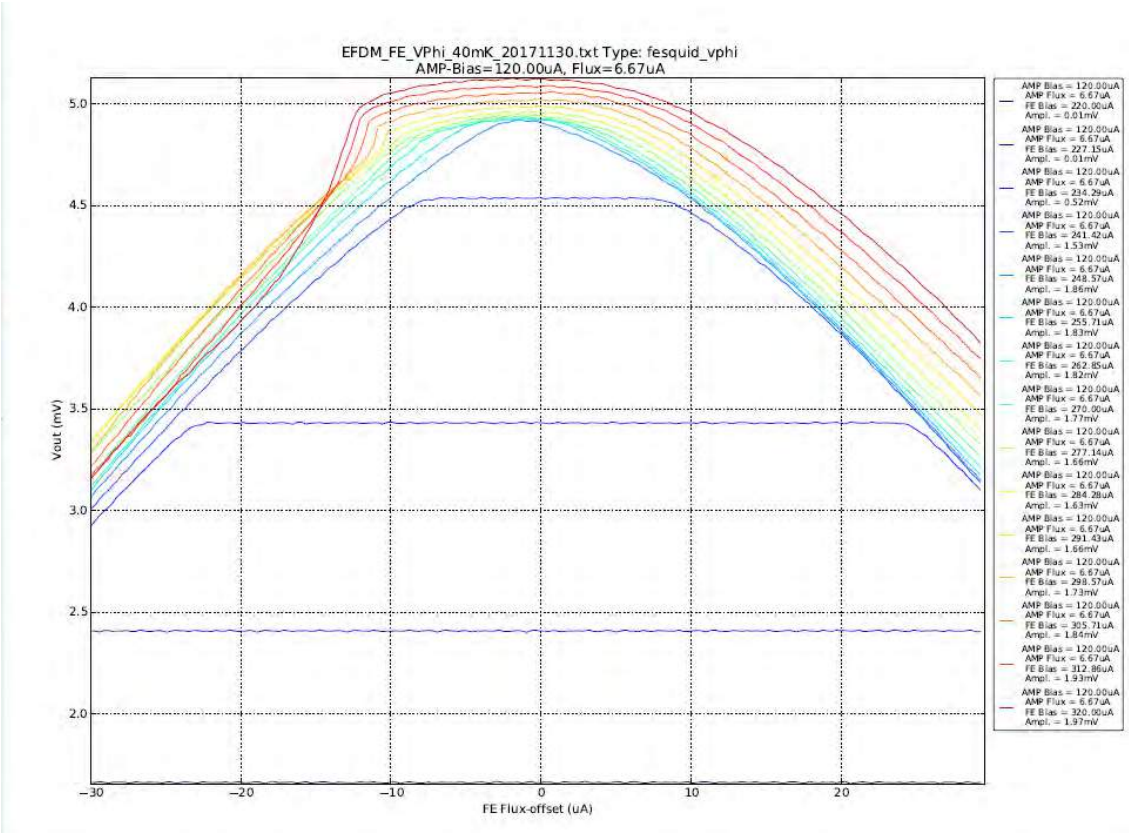



*Figure 10. Input SQUID VPhi curve, measured in run 67 with snubber, SC-shield and FB-resistance divider of FEE6.*

What can be seen is that between run 66 and 67 there are still Empuku oscillations occurring in the SQUID (Figure above, at -15 to -10 uA flux offset current).

This measurement will be repeated upcoming run, without the FB-divider in place, in order to get a 1-to-1 comparison for the Noise measurement data. Now the calibration signals differ significantly between the two measurements of run 66 and 67.