AHEAD ***Integrated Activities for the High Energy Astrophysics Domain*** ***H2020-INFRAIA-2014-2015, grant 654215***	**Deliverable 6.4 'New set of SQUIDs for readout'**	***DATE: 28/09/2017*** ***PAGE:*** *1 of 12*

Title	**SQUID fabrication and test**		
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Agreed by :		Date :	
Authorised by:		Date :	

Distribution:

Document Change Record

Issue	Date	Changed Section	Description of Change
ESA-CTP TN 8.5, issue 0.9	7 July 2017	All	Version of document submitted to ESA for milestone review
AHEAD D 6.4	28 August 2017	Section 5	Section 5 added, AHEAD-specific document title inserted
AHEAD D 6.4	28 September 2017	Section 1	A missing sentence added

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1 BACKGROUND

A set of SQUID devices for the baseline X-IFU readout chain has been designed within the project at hand, the ESA-CTP[1], as well as a number of more ambitious SQUID devices for the alternative readout chains within the EU-AHEAD[2] project. The device designs have been covered in Technical Note 2.4 "SQUID design update" Issue 2.1, dated November 14th 2016. The latter set of SQUIDs constitute the deliverable D6.4 of Workpackage WP6.3 of the ATHENA project.

The goal of this work has been to prepare for the SQUID readout chain of the X-IFU Demonstration Model, where multiplexing factor 40 is aspired. Because the finnish national funding application to TEKES (submitted in spring 2015) was not successful, it may turn out to be necessary to find the the SQUID chain for the Demonstration Model either from the wafers described here, or from the upcoming ESA CTP II -project whose proposal was submitted on July 4th 2017. Along with the successful operation of the X-IFU Demonstration Model, the SQUID chain would reach the TRL 5 maturity level.

This document is an amended version of Technical Note 8.5, issue 0.9 (dated 7th July) submitted to the ESA CTP-pixel project. The amended part describes the SQUID device designs specific to the AHEAD project, which were processed on wafers shared between the ESA CTP and AHEAD.

2 FABRICATION PROCESS

The devices have been fabricated using a process[3] with 11 mask layers and the main constituent elements:

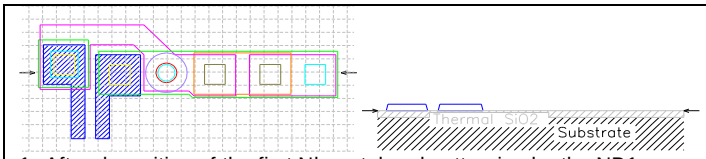
	VTT process
Lithography	Canon FPA3000-i4 projection stepper, 0.35 μm resolution, 0.1μm alignment
Substrate	150 mm Si wafer, thermally oxidized
1st wiring	200 nm Nb
1st insulation	300°C PECVD SiO_2 , proprietary double deposition, 250 nm final thickness
2nd wiring	Base electrode of the whole-wafer trilayer, 250 nm Nb remains after JJ – defining etch
Josephson junctions	Counter electrode of the trilayer, 10/70nm Al-AlO_x/Nb. RIE patterned, light surface anodization
2nd insulation	180°C PECVD SiO_2, proprietary double deposition, 270 nm final thickness
Resistors	TiW 4Ω/□
3rd insulation	100 nm 180°C PECVD SiO_2
3rd wiring	350 nm Nb
Bonding metal	Currently none on wire bond pads, Au on probe contact pads
Passivation	450 nm SiO_2
Cooling fins	400 nm Au

[1] TES Detector Development for Athena / X-IFU, Optimization of a European Transition Edge Sensor Array
[2] Integrated Activities for the High Energy Astrophysics Domain
[3] *IEEE Transactions on Superconductivity*, DOI: 10.1109/TASC.2016.2544821

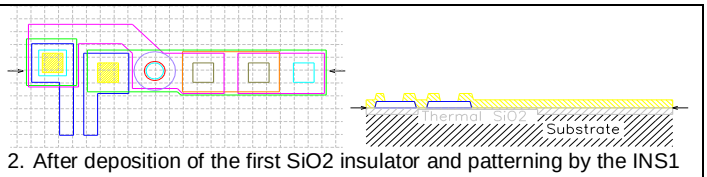
The mask layers are in their order of use:

Mask name	Description
NB1	First wiring
INS1	Vias in first isolation to NB1 layer
CER	Trilayer counterelectrode
ANOD	Sidewall anodisation
NB2	Trilayer base electrode / second wiring
LATR	Vias for capacitors
RES	Shunt resistor
INS3	Vias to RES layer
INS2	Vias to JJ tops and NB2 layer
NB3	Third wiring
PASS	Passivation, bond pad metallization
AU	Cooling fins

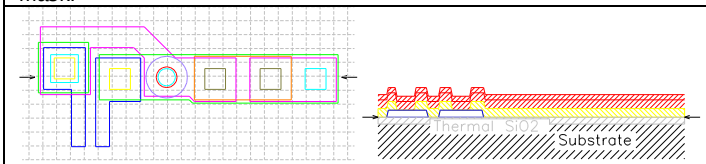
The thin film stack is formed in the following order, the data taken from the E-SQUID design rules version 2.1. The ESA CTP fabrication round additionally includes on-chip capacitors, passivation, and Au cooling fins. Au also acts as the contact metal at pads intended for reticle-level testing. Capacitors were lost from the FAB when the VTT process moved from the non-CMOS-clean M2 part of the VTT clean room into the CMOS-clean M1 part, after the TRP5417 project. Re-introduction of the capacitors became important when it turned out that the back-action noise of the SQUIDs is going to be a significant contribution to the noise budget. The capacitors are used in series with microwave-damping resistors; they block the Johnson noise at signal frequencies, but still allow the damping circuitry to function at several gigahertz where Josephson oscillation occurs.



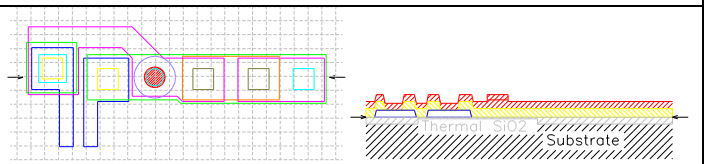
1. After deposition of the first Nb metal and patterning by the NB1 mask.



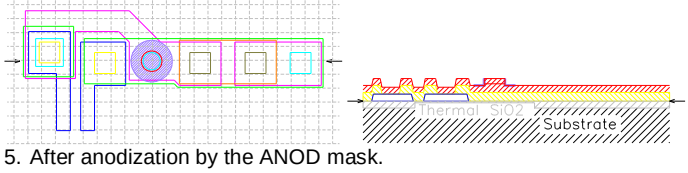
2. After deposition of the first SiO2 insulator and patterning by the INS1 mask.



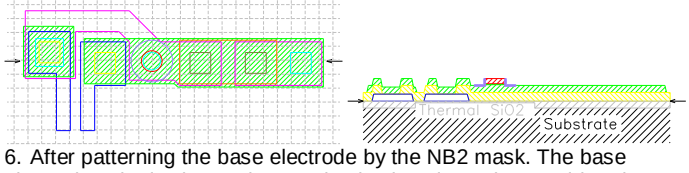
3. After deposition of the Nb/Al-AlOx/Nb trilayer.



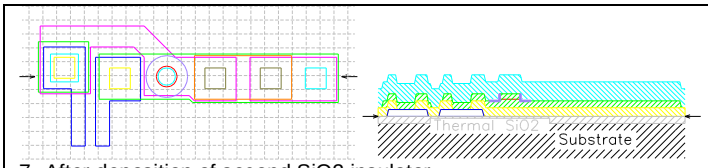
4. After patterning the counterelectrode by the CER mask.



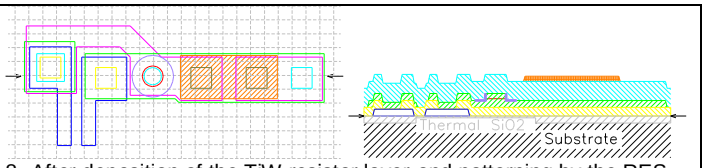
5. After anodization by the ANOD mask.



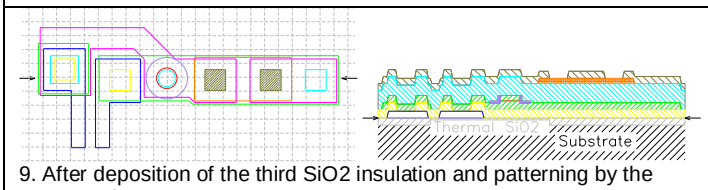
6. After patterning the base electrode by the NB2 mask. The base electrode color is changed to emphasize how it can be considered as the second Nb wiring layer.



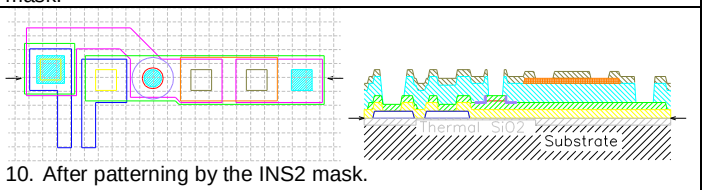
7. After deposition of second SiO2 insulator



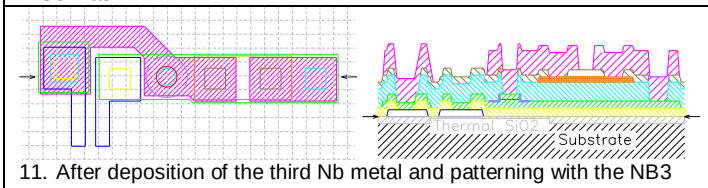
8. After deposition of the TiW resistor layer and patterning by the RES mask.



9. After deposition of the third SiO2 insulation and patterning by the INS3 mask.



10. After patterning by the INS2 mask.



11. After deposition of the third Nb metal and patterning with the NB3 mask.

In addition to the E-SQUID process flow:

- Capacitor dielectric is formed on the designated areas of the surface of the lower niobium, the niobium being the remaining base electrode of the Nb/Al-AlOx/Nb trilayer after the CER etch (step 4). The Nb_2O_5 dielectric is formed by anodization in the step 5. Because the Nb_2O_5 does not stop plasma etching through the SiO_2 insulators well, a separate wet etch is performed after step 7 to open a via in the second SiO_2. In the step 8 a TiW plate will land on top of the Nb_2O_5 dielectric, where it will act as an etch stop for subsequent plasma etch steps, and as the capacitor top electrode. A big INS3 via is opened to the TiW plate in step 9, and the third niobium deposited in step 11 will land on the TiW and proximitize it into superconductive state.
- After the step 11 SiO_2 passivation layer is deposited, and contact windows opened to (i) bond pads, and to (ii) resistor areas designated as cooling fins. Because the PASS patterning is performed with contact lithography, rather than projection lithography, also reticle codes are etched to chips during this step.
- After the passivation step, gold is deposited and lift-off patterned to create the electron-phonon coupling volumes (cooling fins) on top of the resistors.

3 FABRICATION STATUS

As of June 30th two wafers have been finished:

- ATH#4, targeted for medium critical current density, but lacking the SiO2 passivation and Au cooling fins.
- ATH#1, targeted for low critical current density, and equipped with passivation and gold.

Owing to malfunction of the film thickness meter, it was not clear whether the PASS etch had left a few nanometers of unetched SiO_2 or not, which on the pads would get penetrated by wire bonding, but which might impede the cooling effect of the Au fins. Hence we decided to finish the wafer ATH#4, whereby we could test the Au-TiW contact electrically from monitor chips, but leave the other wafers in storage, to be able to perform the conceivable overetching step.

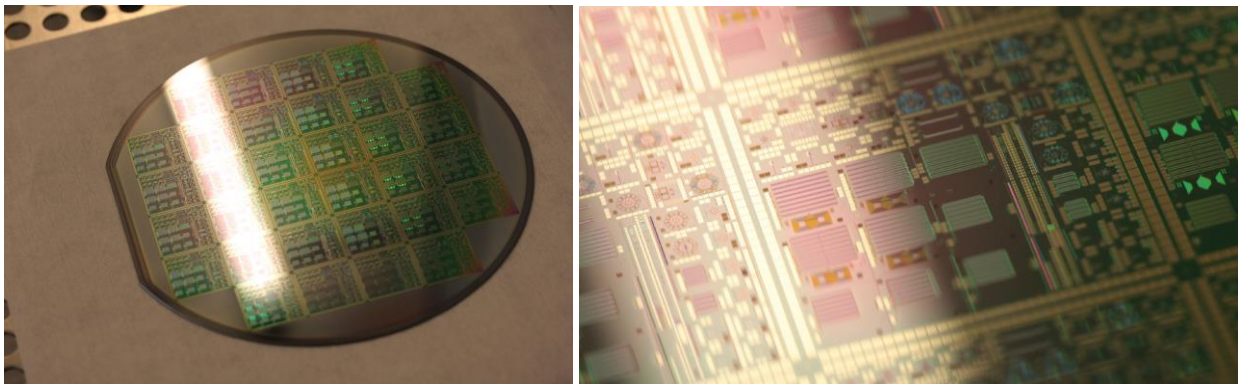


Figure 1: (Left) The wafer ATH#4 as of June 7th, (Right) Close-up of one reticle field on the wafer.

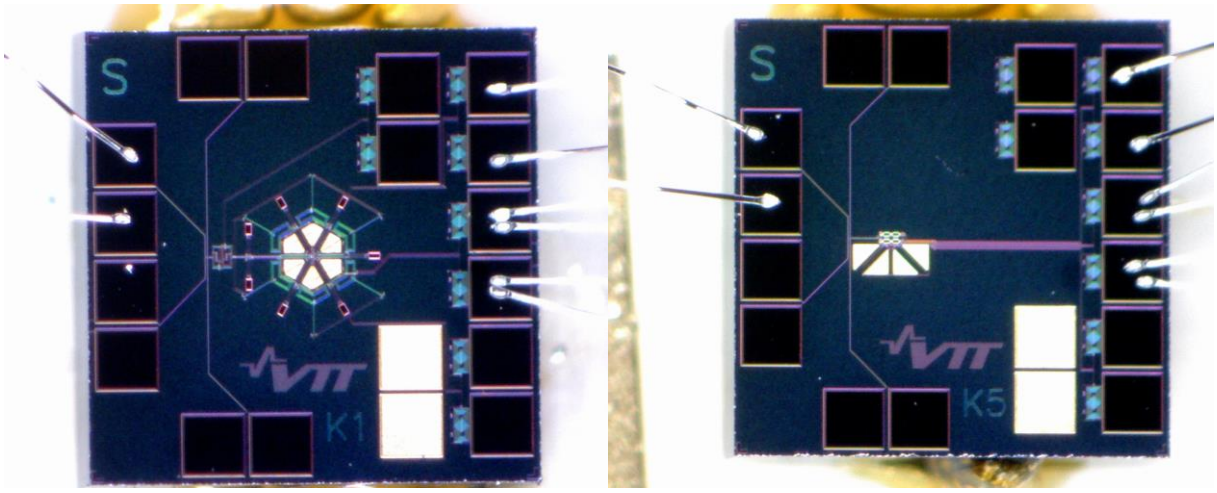


Figure 2: (Left) Microphotograph of a K1 front-end SQUID as of June 30th, and (right) a K5 front-end SQUID from wafer ATH#1. The gold-plated thermalization pads and cooling fins appear brighter than the bonding pads with niobium surface.

3.1 Process continuation plan

The remaining wafers are semi-finished in storage, and will be finished on as-needed basis. The wafers ATH#2 and ATH#3 have been fabricated at the medium critical current density as target, but different thicknesses of the Nb_2O_5 anodized layer. These include zero thickness in the wafer ATH#2, which would produce shorts instead of capacitors, and which could be utilized in case the capacitors fail to operate in the intended manner.The ATH#5 wafer has been targeted for a high critical current density.

4 TESTING

4.1 Some SQUID test in liquid helium at 4.2 K

A handful SQUID devices from the wafers ATH#1 and ATH#4 have been tested, and some characteristics are shown below. Scales on the plots will need to be verified. The first impression is that the fabrication round was successful. It is too early to estimate the realized parameters and their variation, but in general they seem roughly correct. In the two-SQUID configuration the FE+AMP SQUIDs have exhibited instabilitiy whose remedy is underway. Reliable noise estimates for the FE SQUIDs can be expected only when the two-SQUID setup is stable. In addition to the SQUID behaviour, we have verified that the nominally 0.5 mΩ resistor onboard the K4 chip functions and has roughly correct resistance.

The tested SQUIDs include the L1 and L3B arrays intended as boosters, where L3B is a test subtype of L3 with additional microwave damping. The K4 -type 6-series arrays intended for antiCO detector were also tested, as well as the K1- and K5-type front end SQUIDs. The FE SQUID noise performance has not yet been verified.

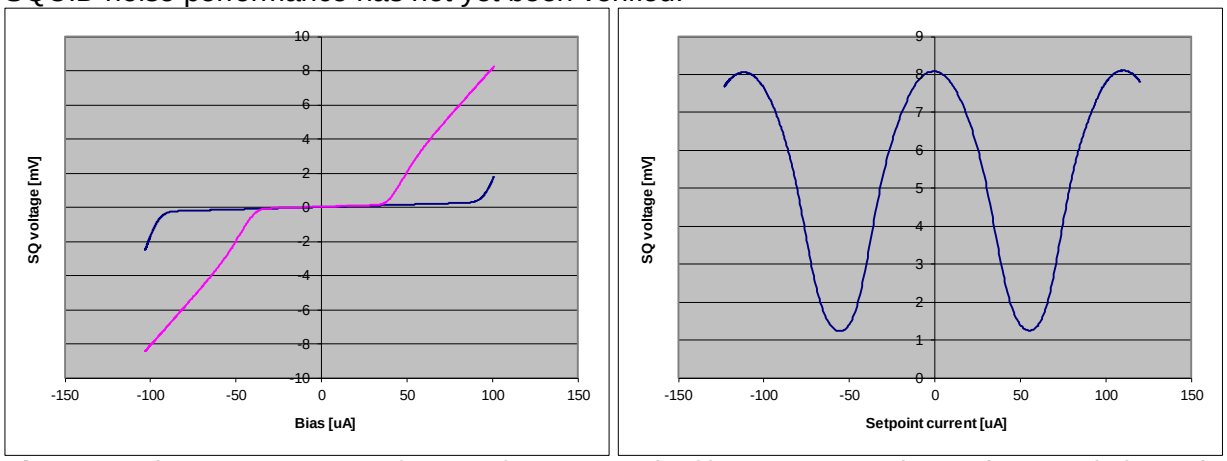


Figure 3: The K3B type, retG from wafer ATH#4. (Left) Currnet-to-voltage characteristics at integer and half-integer flux. (Right) Flux-to-voltage characteristics via SETP coil, at close to maximum modulation depth.

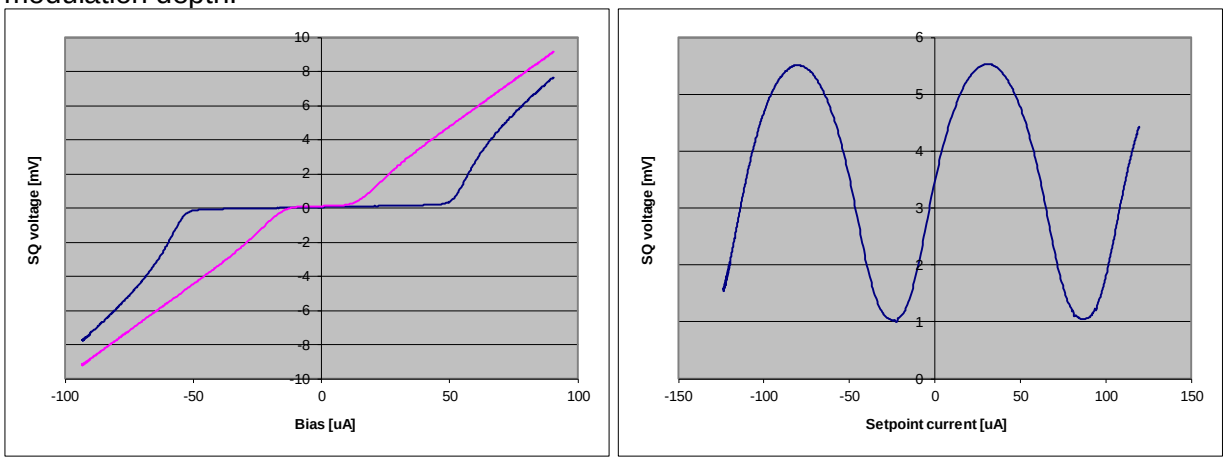


Figure 4: The K3B type, retM from wafer ATH#1. (Left) Currnet-to-voltage characteristics at integer and half-integer flux. (Right) Flux-to-voltage characteristics via SETP coil, at close to maximum modulation depth.

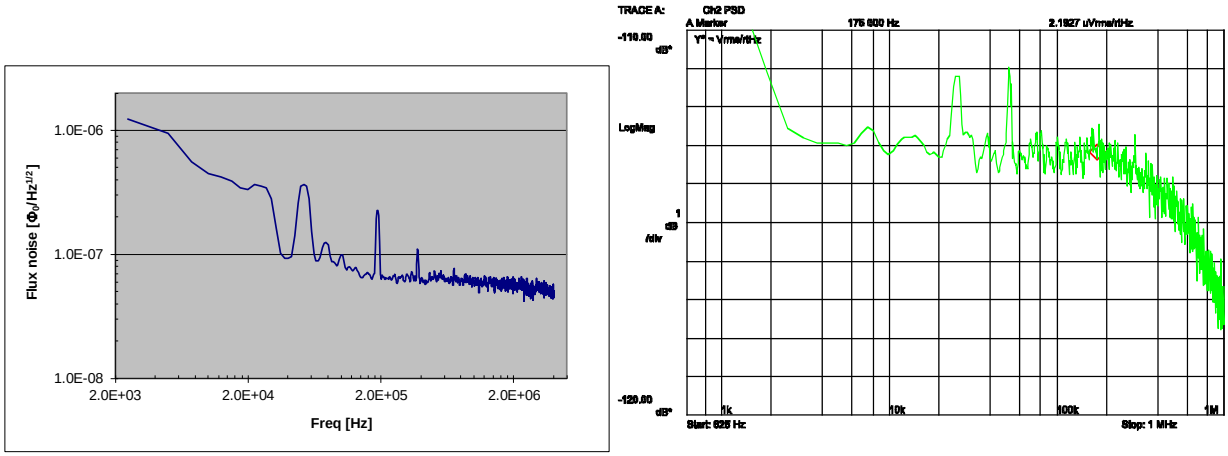


Figure 5: (Left) The K3B type, retM from wafer ATH#1, observed flux noise. (Left) Currnet-to-voltage characteristics at integer and half-integer flux. (Right) The K3B type, retG from wafer ATH#4, a nominally 1 Ω resistor connected across input. The observed white current noise suggests the resistance of 0.8 Ω at 4.2 K, and corner frequency the SQUID input inductance of L_{IN} = 160 nH.

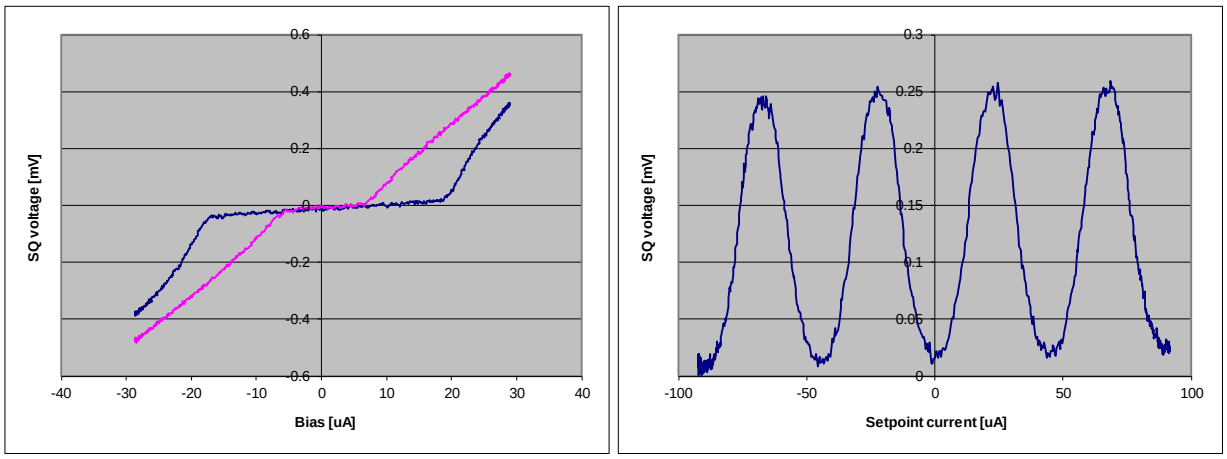


Figure 6: The K4 type, retG from wafer ATH#4. (Left) Currnet-to-voltage characteristics at integer and half-integer flux. (Right) Flux-to-voltage characteristics via SETP coil, at close to maximum modulation depth. The visible ripple is due to the rms noise caused by the very wideband LNA.

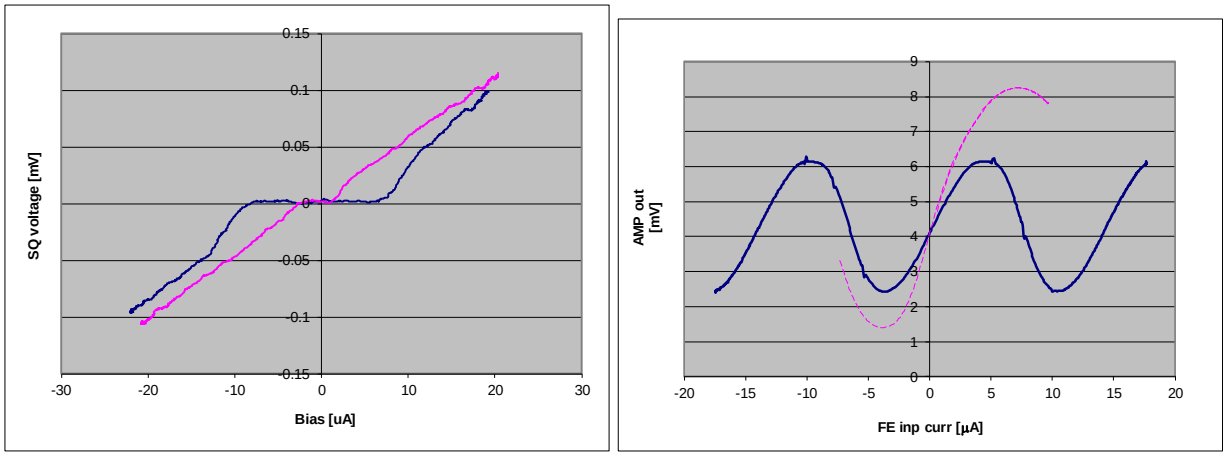


Figure 7: The K1 type, retG from wafer ATH#4. (Left) Currnet-to-voltage characteristics at integer and half-integer flux. (Right) Flux-to-current characteristics of a K5 type SQUID, retM ATH#1, when its current is measured by a L3B retG ATH#4 second stage. The K5 is driven via input coil. The L3B slope, through which the amplification occurs, is also shown in purple (horizontal axis is not valid for the L3B current, the L3B turnpoint-to-turnpoint current range is ~ 18 μA).

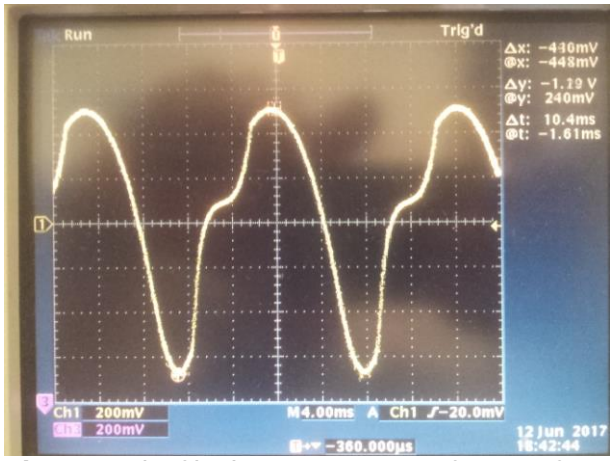


Figure 8: (Left) The L1 type, retG from wafer ATH#4: functioned, but showed Enpuku-style plateaus. It has not yet been investigated whether the plateaus were intrinsic to the device, or a result of mis-wiring or some other mistake.

4.2 Deliveries

As of 7th July 2017 we have delivered five chips to SRON: L3B retS, K1 retM and K5 retM from wafer ATH#1; L3B retG and K1 retG from wafer ATH#4. Their functioning has been verified in LHe.

We have also delivered to INAF/IAPS three chips of the K4 type: retM and retS from wafer ATH#1; and retG from wafer ATH#4. Other chips have been verified in LHe, except the retS#1 which is untested.

5 AHEAD-SPECIFIC DESIGNS

As described in the document TN 2.4 "SQUID design update", the ESA-CTP specific designs are intended for the 2-stage cryogenic readout chain, which consists of a front end SQUID at 50 mK temperature in vicinity of the main TES array, and a cable-driving booster SQUID at 2.5 K. Additionally, there is a 50 mK single-stage readout chain intended for the anti-coincidence detector. The AHEAD specific SQUID devices were intended for more novel readout concepts: (i) Hi-Z sumpoint, (ii) 300 mK front-end, (iii) local linearization and (iv) 3-stage readout chain.

- The Hi-Z sumpoint attempts to avoid the inductive parasitics, which must stay at nanohenry or sub-nanohenry level when the TES setpoint resistance is as low as 0.025 Ω (SRON designs) or 0.007 Ω, (NASA-GSFC designs). This is achieved by using a step-up transformer very close to the TESes. The transformer can be inductive[4] or capacitive[5] and the SQUID can be located either at 50 mK or at 300 mK.
- The 300 mK front-ends attempt to locate the first SQUID amplifier at higher refrigerator temperature, where there is more cooling power available.
- Local linearization attempts to increase the linearity and dynamic range by applying local flux feedback on the SQUID. This would relieve the system-level requirements on the Baseband feedback (BBFB).
- Three stages would provide more power gain that the baseline two-stage chain. This approach would redeem some of the power gain lost due to local linearization.

Division of the chip designs by their intended use is shown in the Table below:

ESA-CTP -specific designs:			
Chiptype designation	*Derived from E-SQUID chiptype...*	*Target*	*Main features*
K1	G1	50 mK front end, main TES array	6-multiloop single SQUID, ultra-small 1.8 um Josephson junctions, for improved interstage bandwidth
K4	G3	50 mK. anti-conincidence detector	6-series SQUID array, integrated milliohm-resistors for anti-CO biasing
K5	new	50 mK front end, main TES array	2-series array, for improved interstage bandwidth. Beta-C reduced in order to meet 50 mK compatible power dissipation.

[4] M. Kiviranta et al., *Proceedings of far-IR, sub-mm & mm detector technology workshop*, 1-3 April 2002, Monterey, California, Figure 5.
[5] P. de Korte et al., *7th International workshop on low temperature electronics*, 21-23 June 2006, Noordwijk, the Netherlands.

K6	G1	- "" -.	K1 without capacitive dc-blocks in microwave dampers. Fallback device in case capacitor fabrication fails.
L1	new	Booster, main TES array	128-series 3-parallel SQUID array. Lower-L_{IN} version of L3 to improve interstage bandwidth
L3	F5	- "" -	184-series 4-parallel SQUID array
L4	F5	-""-	Version of L3 with inverted loop polarities, by Damien Prele's suggestion to implement the LNA topology of ref[6]
AHEAD -specific designs			
Chiptype designation	*Derived from E-SQUID chiptype...*	*Purpose*	*Main features*
K2	G2	Locally linearized	K1 equipped with 1:12 intermediate transformer, low-Z input, hi-Z local feedback
K2B	G2	Hi-Z sumpoint	K1 equipped with 1:12 intermediate transformer, hi-Z input
K3	G3	300 mK front end	6-series SQUID array
K7	G7 (G2)	Locally linearized	K1 equipped with 1:6 intermediate transformer, low-Z input, hi-Z local feedback
K7B	G7 (G2)	Hi-Z sumpoint	K1 equipped with 1:6 intermediate transformer, hi-Z input
L2	new	Three-stage	50-series SQUID array. For general-purpose experimenting, or as an intermediate stage of 3-stage readout chain.
L5	G5	Three-stage	Bias-reusing chip; integrates 2nd and 3rd stage of the 3-stage readout on single chip¨.

6 SUMMARY

The fabrication round in general appears successful.

[6] D. Drung et al., *IEEE Tran. Appl. Supercond.* **23** (3) 1100204, June 2013.