

AHEAD2020 deliverable WP15.8 TES array chips and relevant auxiliary chip set Project acronym: AHEAD2020 Project Title: Integrated Activities for the High Energy Astrophysics Domain Grant Agreement No: 871158 This deliverable is part of a project that has received funding from the European Union's Horizon 2020 research and innovation programme Start date of the project: 2020-03-02

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TABLE OF CONTENTS

1.	SUE	BJECT	4
	1.1	Acronyms list	4
2.	APF	PLICABLE AND REFERENCE DOCUMENTS	5
	2.1	Applicable Documents	5
	2.2	Reference Documents	5
3.	INT	RODUCTION	6
4.	TES	CHIPS	7
5.	LC	FILTER CHIPS	11
6.	SQI	JID CHIPS	14
	6.1	FE SQUID stage:	.14
	6.2	AMP SQUID	.15



1. SUBJECT

This document reports the set of chips that are available for the implementation of the TES X-ray spectrometer prototype to be realized in the frame of the AHEAD2020 project WP15.

1.1 Acronyms list

ADC	Analog to Digital Converter
ADR	Adiabatic Demagnetization Refrigerator
AHEAD	integrated Activities for the High Energy Astrophysics Domain
AIV	Assembly Integration and Verification
CFEE	Cold Front End Electronics
DAC	Digital to Analog Converter
DR	Dynamic Range
EC	European Commission
ESA	European Space Agency
ETF	Electro Thermal Feedback
EU	European Union
FEE	Front-End Electronics
FDM	Frequency Division Multiplexing
FWHM	Full Width at Half Maximum
FLL	Flux Locked Loop
FOV	Field Of View
ICD	Interface Control Document
LNA	Low Noise Amplifier
PCB	Printed Circuit Board
PIXE	Particle Induced X-ray Emission
P/L	Pavload
QE	Quantum Efficiency
SQUID	Superconducting Quantum Interference Device
SRON	Space Research Organization of Nederland
SpW	SpaceWire
TAS	Thales Alenia Space
TAS-I	Thales Alenia Space-Italia
TBC	To Be Confirmed
TBD	To Be Defined
TBV	To Be Verified
TBW	To Be Written
TES	Transition Edge Superconductor
TDM	Time Division Multiplexing
TM/TC	TeleMetry and TeleCommand
WBEE	Warm Back End Electronics
WFEE	Warm Front End Electronics
WP	Work Package
	<u> </u>

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2. **APPLICABLE AND REFERENCE DOCUMENTS**

Applicable Documents 2.1

AD1: Grant Agreement number: 871158 — AHEAD2020 H2020-INFRAIA-2018-2020/H2020-INFRAIA-2019-1

2.2 **Reference Documents**

RD1: Detailed design requirements of the TES spectrometer AHEAD2020 deliverable D15.6, TASI-STU-0111, issue1, August 2021





3. INTRODUCTION

The deliverable item D15.8 for the project AHEAD2020 is constituted by a set of TES array detector and the related chipset (the LC filters and SQUIDs) to be used in the development of the TES X-ray spectrometer which is the object of WP15.2.

The details about the TES X-ray spectrometer can be found in RD2, herebelow is shown sketch of the spectrometer cold head showing the use of the various chips.



Fig. 3.1: sketch of the Detector Holder, Cold Finger, Secondary Cold Finger (only conceptual not truly representative nor to scale w.r.t the actual design)

The following pages give evidence of the chips that have been selected and are presently kept in safe storage at the SRON clean room ready for integration on the spectrometer when needed.

This document is used to close the deliverable D15.8 task.



4. TES CHIPS

There are several options for TES array chips that are all from the same fabrication run on wafer 3 with Tc of 80-90 mK. These are all 8x8 arrays and upper half (North) or lower half (South) part of the chips can be wired for 32 pixels array.

The chips on this wafer are named as M followed by a number#.

- TES size: 80x20 µm²
 - o Chip M6 South
 - Chip M6 North





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The following combination was tested in the SRON lab:

TES array: Wafer 3 Chip M6, 8x8 array 80x20 um2, south side connected (32 pixels)

Transformers: SC13-1 Chip 14a, coil ratio 1:1.125, k = 0.92

LC filters: LC20-2 Chip 3, 4 uH coil (Leff = 3.6 uH), spiral return design

This is tested in the XFDM setup in late 2020, when we demonstrated 2.38 eV with 32 MUX.

We were using 4 uH + 1:1.125 transformer. Not using the transformer (so 4 uH effective inductance) will slightly spoil the performance but given that the requirement is 15 eV FWHM this configuration is possible.



Fig. 4.2: The spectrum of each 32 TESs taken simultaneously using FDM readout.





Fig. 4.3: The combined spectrum of 32 TESs MUX measurements using FDM readout.

Other options for TES chips are:

- TES size: 80x13 µm² _
 - M1 North 0
 - M2 North 0
 - M3 South 0
 - M4 South \cap

M1 South was tested with the same transformer and LC filter and performed even better than M6. The result is accepted now for publication in APL.

The summed X-ray spectral resolutions @ 5.9 keV is 2.14 eV for 31 pixels MUX.





Fig. 4.4: The combined spectrum of 31 TESs simultaneous measurements using FDM readout for M1 South (80x13 µm² TESs).



5. LC FILTER CHIPS

4 LC filter chips are considered to be used with the following numbers:

- LC20-1 Chip 3
- LC20-1 Chip 7
- LC20-2 Chip 3
- LC20-2 Chip 3

Chip dimensions:	20.0 x 16.5 mm ²
Organization:	32 channels, in a 4 x 8 array (see Fig. 5.2.2)
Resonance frequencies:	1 to 5 MHz (100 kHz spacing)
	$L = 4 \ \mu H$ for all channels

LC20-2 Chip 3 has been used and tested with the first set TES option mentioned above.

There are 32 resonators from 1-5 MHz as shown below with high Q-factors and small series resistances.



Fig. 5.1: LC20-2 chip 3: 32 LC filter resonators from 1 to 5 MHz.





Fig. 5.2: LC20-2 chip 3, resonance frequencies and the deviation from the linear trend.



Fig. 5.3: LC20-2 chip 3, Q factors and the deviation from the linear trend.





Fig. 5.4: LC20-2 chip 3 and M6 South 32 pixels wired for test.





6. SQUID CHIPS

The envisaged RES spectrometer described in RD2 foresee two SQUID stages, a preamplifier SQUID dubbed FE SQUID mounted on the primary cold finger working at < 100 mK and an amplifier SQUID dubbed AMP SQUID mounted on the secondary cold finger working at 1 K.

6.1 FE SQUID stage:

These are the two options for Front End (FE) SQUID:

- M1B retG CTP7
- M1B retM CTP7



Fig. 6.1.1: Picture of an M1B SQUID.





6.2 AMP SQUID

These are the options for AMP SQUIDs:

- L1X retF ATH5
- L1X retT ATH3

Fig. 6.2.1 & 6.2.3 shows some I-V curves of the L1Xret4 ATH5 (so not exactly the one we intend to use but same batch), and the constructed V-Phi curve from the 120 Ω load line.



Fig. 6.2.1: I-V curves of the L1Xret4 ATH5 and the 120 Ω load line.



Fig. 6.2.2: V-phi curve constructed through the 120 load line. Periodicity = 32uA/phi0.





Fig. 6.2.3: picture of an L1X SQUID under test.

END OF DOCUMENT

