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Superconducting Multilayer High-Density Flexible Printed Circuit Board for Very High Thermal Resistance Interconnections

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Abstract We have successively developed two superconducting flexible PCBs for cryogenic applications. The first one is monolayer, includes 552 tracks (10 μm wide, 20 μm spacing), and receives 24 wire-bonded integrated circuits. The second one is multilayer, with one track layer between two shielding layers interconnected by microvias, includes 37 tracks, and can be interconnected at both ends by wire bonding or by connectors. The first cold measurements have been performed and show good performances. The novelty of these products is, for the first one, the association of superconducting materials with very narrow pitch and bonded integrated circuits and, for the second one, the introduction of a superconducting multilayer structure interconnected by vias which is, to our knowledge, a world-first.

Keywords Superconducting flexible PCB · Cryo-electronics · Cryogenics

1 Context, Needs, and Solution

Many ultra-sensitive detectors, such as IR, X-ray or dark matter detectors, operate at deep cryogenic temperatures, and the number of space detectors requiring such temperatures increases. For example, we are involved in the development of several space instrument projects that all implement arrays of cryogenic detectors: X-IFU [1] for the Athena satellite (an X-ray spectro-imager of 3840 pixels (249 μm pitch) using transition edge sensors (TES)), SAFARI-POL [2] for the SPICA satellite (an IR multi-polarization imager of 1344 pixels (750 μm pitch) using quadruple Si-doped

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sensors), and MicroCal-X [3] (an X-ray spectro-imager of 4096 pixels (500 μm pitch) using Si-doped sensors).

The number of channels of these kinds of detectors being always increasing, this causes ever greater difficulties in extracting the signals from the detector. Indeed, each electrical link generates thermal leaks that multiply with the number of interconnections, until it becomes impossible to cool down the detector because the cooling power of the cryogenerator is insufficient. For example, space cryogenerators can evacuate only a few microwatts at 50 mK, and in conventional technology (copper or manganin) this limits the number of readout wires to a few hundred at most. So new interconnection technologies become necessary, for needs that are common to many experiments: (1) need to interconnect cold detectors (typically 50–300 mK) with warmer stages (typically 2.5–4 K) containing cryo-electronics, or simply a thermal contact with an intermediate temperature source; (2) need to readout highly segmented detectors (typically 4000-pixel cameras), and so to implement thousands of signal tracks; (3) need to minimize the thermal load on the coldest stage, even in cases where shielded signal lines are required.

To meet this demand, we have developed high-density flexible PCBs, combining the advantages of niobium (for tracks) that is superconducting below ~ 9.3 K and so is an excellent thermal insulator, and the advantages of polyimide (for mechanical support) that has also an intrinsically low thermal conductivity (1.17×10^{-4} W/K/cm) and remains flexible even at very low temperatures. Minimizing in addition the flex section (by implementing very thin polyimide support (17 μm), very thin tracks (350 nm), and very narrow tracks (down to 10 μm) allowing a narrow PCB), we are able to minimize the global thermal conductance of the flex.

From this base, we have successively developed two new products, both in the context of X-ray spatial spectro-imagery. The first product (Sect. 2) receives multiplexing and pre-amplifying chips implemented directly on the flex, in order to benefit from the very large integration level permitted by the narrow tracks, and to simplify the interconnections by reducing the number of output signals. The second product (Sect. 3) appends additional layers on both faces, interconnected by microvias, where shielding grids and thermal contacts are implemented. Both realizations are under characterization, and the first measurements are presented in Sect. 4, including electrical and thermal measurements.

2 First Realization: Monolayer Flexible PCB with Chips on Flex

The first product that we have developed is for the X-ray spectro-imager of our R&D project “MicroCal-X,” where the detector is made of four arrays of 1024 pixels cooled at 50 mK, each pixel forming an unit microcalorimeter. In this system, our flexible PCB has two functions: (1) interconnection of the detector (50 mK) to the readout cryo-electronics (2.5 K) from a plate (300 mK) where the detector is hybridized; (2) implementation of the pre-amplifying and multiplexing cryo-electronics [4].

To perform these two functions, the flexible PCB includes two zones (see Fig. 1). (1) The first zone (left half of the PCB) is the thermal gradient zone, for the progressive passage from 300 mK to 2.5 K. It includes 552 high thermal resistivity superconducting

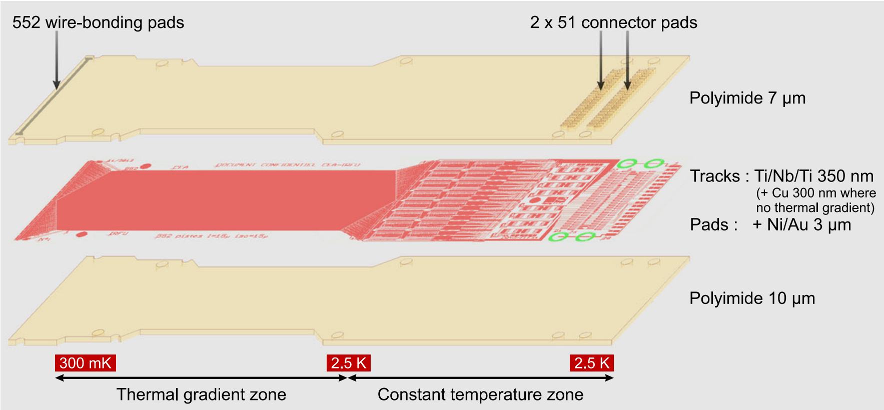

Fig. 1 Stack-up of the layers of the flexible PCB, with their depth and the location of the two functional zones (Color figure online)

tracks that bring the input signals from the detector side (left) to the cryo-electronics side (right). The width of each track is 10 µm, and the space between them is 20 µm. (2) The second zone (right half of the PCB) is the constant temperature zone, where 24 wire-bonded integrated circuits are mounted, on an area of only 23 mm $\times$ 16 mm, and maintained at 2.5 K. In this zone, the superconducting tracks are copper-plated in order to improve the thermalization of the circuits.

To interconnect this flexible PCB, 552 wire bonding pads are designed at the detector side (left); the pitch between pads is 80 µm, disposed in two staggered columns, resulting in an equivalent pitch of 40 µm. At the output side (right), after the multiplexing performed by the cryo-electronics, a 51-way SMD Nano-D connector (23 mm width) is implemented.

The total dimensions of the flexible PCB are $L \times w = 90 \times 23$ mm, while the dimensions of the gradient zone, where thermal isolation is performed, are $L \times w = 25.83 \times 17$ mm. The depth of the PCB is 17 µm; the detail of the layer stack-up is shown in Fig. 1. Figure 2 shows photographs of the produced PCB, and the result of the first tries of gluing and wire bonding of the integrated circuits. The difficulty is due to their extreme proximity, inducing very small space between the PCB pads and the circuits, as well as between the PCB pads of two nearby circuits. In particular, when bonding a circuit, the bonding tool should avoid to damage the wire bonding of the previously bonded circuit. This requires a very precise gluing of the circuits, the use of the thinnest available bonding tool, and an optimization to find the best bonding parameters. The distance between the center of circuit pads (525 µm) and the external edge of the PCB pads is probably a minimum not to exceed.

The next steps of this development will concern the complete population of the PCB: gluing of the stiffeners at both extremities, implantation and wire bonding of the totality of the integrated circuits, and soldering of the SMD Nano-D connector. Then, the PCB will be integrated in the acquisition chain.

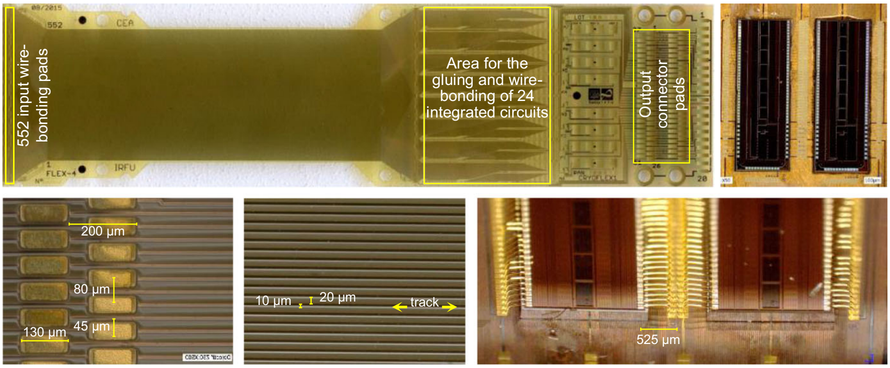

Fig. 2 At top: photograph of the whole PCB (left) and of two circuits before bonding (right). At bottom, left: zoom on the input interconnecting pad area. Middle: zoom on the signal tracks (10 µm width). Right: first try of wire bonding on PCB (right), made difficult by the proximity of circuits (Color figure online)

3 Second Realization: Multilayer Flexible PCB for Shielded Interconnections

The success of this first realization has led us to start a new project, with an additional difficulty: the use of multiple interconnected layers. The aim was to develop generic superconducting harnesses for the readout, in spatial context, of very low impedance detectors (like conventional TES) as well as high impedance detectors (like Si-doped thermometers or high-resistivity TES). These harnesses electrically link pieces at different temperatures, minimizing the thermal conduction between them. A harness contains 37 tracks, routed on a signal layer (see Fig. 3). This one is intercalated between two shielding layers made of hatched shielding planes, and this set is again intercalated between two thermal contact layers where large gold pads are designed at both extremities of the harness and at its middle, for its thermalization at three different temperatures (low, intermediate if needed, and “high”). All the grounds of the four top layers are interconnected by microvias, in order to entirely enclose the lines by shielding and to improve the thermalization. Two interconnection options are available at both extremities: either SMD Nano-D connectors or wire bonding pads if very low contact resistance or maximal compactness is needed.

We have produced four variants of design, with different track widths and spacings: 15, 30, 90, and 300 µm, according to the priority given to specific properties in the considered application: thermal isolation, or critical current, or maximal 300 K track resistance, etc. The characteristics and theoretical performances of each variant are shown in Fig. 4. The length of the harnesses is 100 mm, their maximal width (at connector level) is 19 mm, and their minimal width is given for each variant by the table. Figure 5 shows a photograph of each of the four variants of harness produced, and Fig. 6 shows different details illustrating the quality of the realizations.

The next step of our work will be the implementation of the two kinds of interconnections: the multi-wire bonding if minimization of the contact resistance and the boundary dimensions is needed (after recutting of the PCB at designated locations)

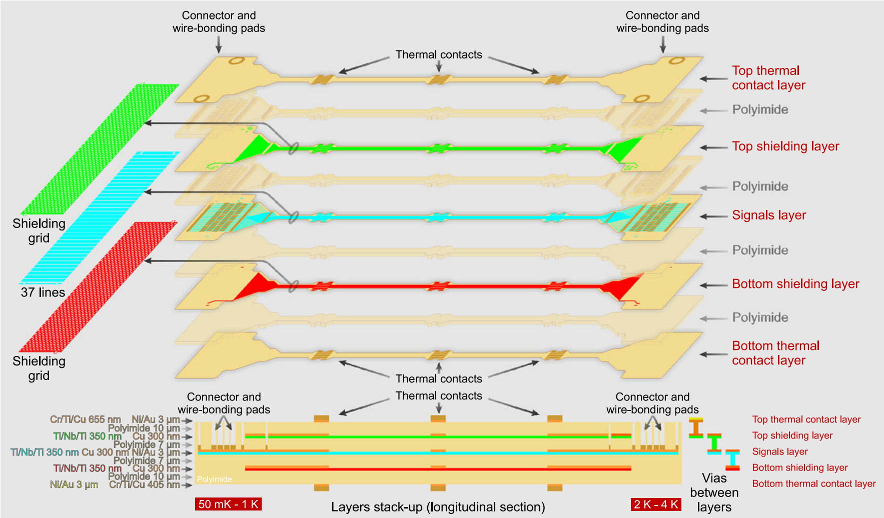

Fig. 3 Stack-up and depth of the harness layers and metallizations (Color figure online)

Characteristics and theoretical performances	Variant 1	Variant 2	Variant 3	Variant 4
Tracks width (µm)	300	90	30	15
Tracks spacing (µm)	100	30	30	15
Shielding filling ratio	0.25	0.5	0.5	0.5
Tracks quantity	32	37	37	37
Minimal harness width (mm)	14.1	5.21	2.99	1.89
Total thermal conduction (W/K)	**1.45E-07**	**6.08E-08**	**2.95E-08**	**1.77E-08**

Fig. 4 Characteristics and theoretical performances for each harness variant (Color figure online)

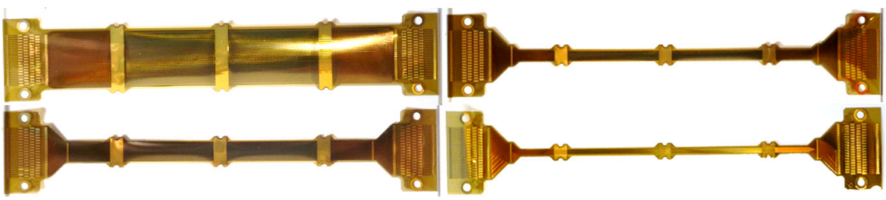

Fig. 5 Photograph of the four harness variants (left: 1 and 2, right: 3 and 4) (Color figure online)

and soldering of the SMD Nano-D connectors. Then, a final version of the harnesses will be produced.

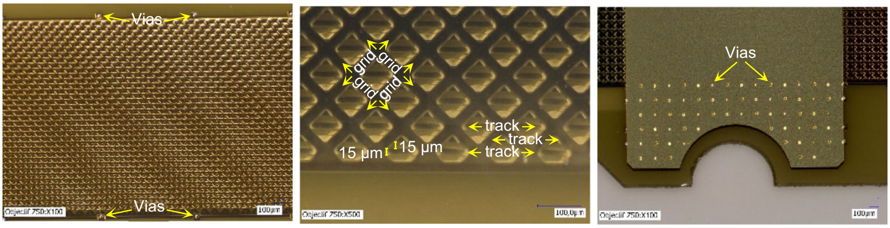

Fig. 6 Left: zoom on the tracks and grids zone (variant 3); the shielding grids are closed by vias. Middle: further zoom (variant 4) where 15 µm/15 µm tracks appear between the two shielding grids. Right: zoom on a top thermal contact, with vias connecting it to the two shielding planes (Color figure online)

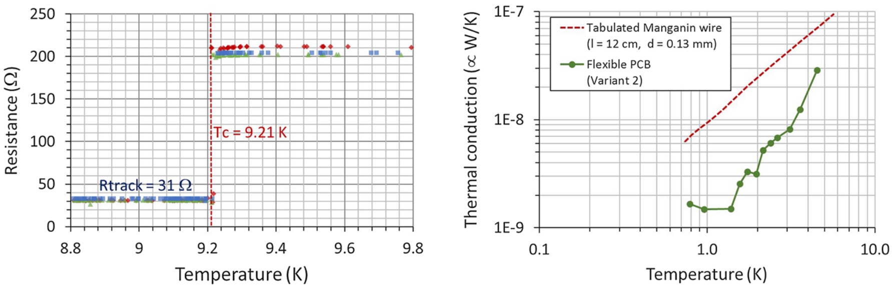

Fig. 7 Left: electrical resistance of three tracks (blue, red, and green) versus temperature: transition around 9.2 K. Right: comparison between the thermal conduction (arbitrary unit) of the Variant 2 of the flexible PCB (thermal insulator area: $w = 5.21$ mm, $L = 2.1 + 2.1$ cm) and the variation of the tabulated values of a manganin wire ($\varnothing = 0.13$ mm, $L = 12$ cm) (Color figure online)

4 Measurements

The critical temperature of the tracks has been measured, by performing a four-wire measurement of their electrical resistance when the temperature was varying in both directions. For the first realization (i.e., the monolayer flexible PCB), the critical temperature measured is ~ 8.5 K, while for the second realization (i.e., the multilayer flexible PCB) it is 9.0–9.2 K (see Fig. 7, left), i.e., very close to that of the bulk niobium (9.3 K). This excellent result is due to an improvement in the metal deposition quality.

A measurement of the critical current for Variant 3 of the flexible PCB has been tried, from 4.5 to 9 K, but the limit of the instrument has been reached (80 mA), proving that the critical current exceeds this value.

The thermal conduction of Variant 2 of the multilayer flexible PCB has been measured between a low temperature of 50 mK and a high temperature varying from 800 mK to 5 K (see Fig. 7, right). For the moment, the measurement is not absolute, but it can be compared to the variation of conductivity of a manganin wire (length 12 cm, diameter 0.13 mm). The residual-resistivity ratio (RRR) has been also measured and exhibits a value between 3 and 4, which indicates a quite good metal deposition (it has doubled from the first to the second realization).

5 Conclusion

The presented technology exhibits satisfactory yields, and its multilayer superconductive structure is, to our knowledge, a world-first. It has also a great potential for many other applications at K- and mK-temperatures, such as some implementations of quantum cryptography or quantum computing, and superconducting electronics in general.

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